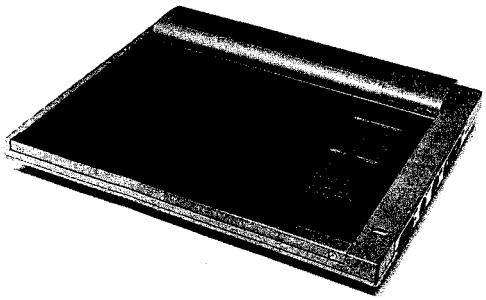
SHARP SERVICE MANUAL

S4005QA-75///



COMPUTER PROJECTION PANEL

MODEL QA-75

In the interests of user-safety (Required by safety regulation in some countries), the set should be restored to its original condition and only parts identical to those specified should be used.

CONTENTS

SHARP CORPORATION

INTRODUCTION

COMPUTER PROJECTION PANEL displays images generated on a personal computer onto a large screen or wall, using an overhead projector as the light source.

QA-75 employs TSTN (Triple Super Twist Nematic) 640 × 480 dot black and white liquid crystal display (LCD). It is designed so that the heat generated by OHP is exhausted from the inside by a fan motor not to increase the temperature of LCD extremely. Approximately DC 12V is supplied as a power source externally through AC adaptor.

Additional functions described below are available by the wireless remote control unit and on the main panel.

① Function to display the pointer (7 × 7 dot or 11 × 11 dot) at an arbitrary position on the screen (POINTER).

② Function of reverse display between black and white (REVERSE).

③ Function to identify colors by an 16-level gray scale (SHADING).

④ Function to identify colors by 16 display patterns (HATCHING).

⑤ Function to fix the display in spite that the image by the computer is changed (FREEZE).

⑥ Function to move the screen (MOVE).

⑦ Function to enlarge the screen (ENLARGE).

In addition, a serial communication terminal (conformable with RS-232C) is equipped with this panel to send signal to a computer. IBM® PS/2, PC/XT/AT (VGA, MCGA, EGA, CGA, MDA, Hercules®/+/In-Color), Apple® II series, and AT & T® (PC6300WGS, PC6386WGS, PC6312WGS, PC6286WGS) are compatible with QA-75. The above functions are not all assured when QA-75 is connected with other computer than the above models.

SPECIFICATIONS

1. SPECIFICATIONS OF MAIN BODY

1.	Display unit	: TSTN LCD
2.	Gray scale of display	: Max. 16 levels
3.	Contrast ratio	: 17:1 (TYPICAL)
4.	Character display area	: Max. about 198 × 148mm
5.	Number of display dots	: 640(W) × 480(H) dots
6.	Dot size	: 0.28(W) × 0.28(H)mm
7.	Dot pitch	: 0.31(W) × 0.31(H)mm
8.	Input video signal	: TTL level – R, G, B, r, g, b, I, Hsync, Vsync or Analog level – VGA signal for IBM PS/2 or Analog level – APPLE MAC II video card signal
9.	I/O connection port	: Video signal input connector (1) Serial port connector (1) DC power input connector (1)
10.	Switch	: DC power ON/OFF switch Function switches (8) Threshold adjustment volume (1)
11.	Function	: Horizontal/vertical adjustment of image position Phase adjustment Frequency adjustment Software RESET Gray scale processing (shading) Hatching RGB select Image reverse processing Image clear processing Contrast adjustment Pointer control Image freeze processing Image enlarge processing Image move Menu display Computer control Remote control

Input video signal automatic discrimination

Adjusted condition retaining function

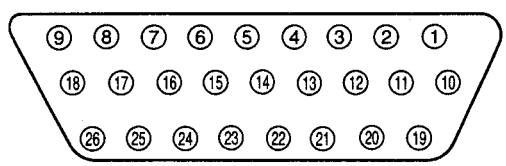
12. Dimensions : 363(W) × 316(H) × 53(D)mm
13. Net weight : Approx. 3kg

2. SPECIFICATIONS OF INTERFACE

2.1. Video signal input selection

Input signal layout :

① Digital Secondary Green (g, I)
② Digital Secondary Blue (b, Video)
③ Digital Secondary Red (r)
④ Analog Blue
⑤ Analog Green
⑥ Analog Red
⑦ Digital GND
⑧ Test 1 (MAC II)
⑨ Test 2 (D/A)
⑩ Digital Green
⑪ Digital Red
⑫ Digital Blue
⑬ Analog Blue Return
⑭ Analog Green Return
⑮ Analog Red Return
⑯ Digital GND
⑰ N.C.
⑱ N.C.
⑲ Vsync (Digital)
⑳ Hsync/Csync (Digital)
㉑ N.C.
㉒ N.C.
㉓ Digital GND
㉔ Digital GND
㉕ Digital GND
㉖ N.C.



TEST 1 terminal : Must be set to LOW (GND) for analog APPLE MAC II video card signal input, and to open (N.C.) for other signal input.

TEST 2 terminal : Must be set to LOW (GND) for analog APPLE MAC II video card signal or IBM VGA signal input, and to open (N.C.) for digital video signal input.

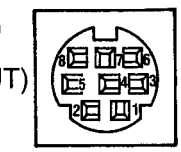
2.2. Power input selection

Input terminal : Center pin + polarity

Input voltage : 12V DC (with main body under load.), 900mA with supplied special AC adaptor.

2.3. Serial interface port

Signal position :
① Signal GND
② Transmitted Data (OUTPUT)
③ Received Data (INPUT)
④ Request to Send (OUTPUT)
⑤ Clear to Send (INPUT)
⑥ Data Set Ready (INPUT)
⑦ Signal GND
⑧ Data Terminal Ready (OUTPUT)



Signal level : Shall conform to the requirement of EIA-232-C standard.

3. SPECIFICATIONS OF ENVIRONMENT

Basically, these environmental specifications apply to the main body and its accessories.

Table 1

Item		Specification	Remarks
Operating environment	Operating temperature	0 to 30°C (The LCD surface temperature shall be 45°C or lower.)	No dew condensation
	Operating humidity	Ta ≦ 40°C : 90% RH Ta > 40°C : Absolute humidity shall be less than Ta = 40°C/ 90% RH (Ta : Temperature of the LCD)	
Storing environment	Storage temperature	−20 to 60°C	
	Storage humidity	Same as the operating humidity condition	

ADJUSTMENT OF P.W.B.

1. ADJUSTMENT OF LCD UNIT CONTROL P.W.B.

This unit involves three adjusting points: VR1 to vary the internal power source V_{CPU} and V_C; L15 to vary the operating point of Low Band VCO; and L14 to vary the operating point of High Band VCO.
This unit does not operate normally unless these points are adjusted properly. Adjustment and readjustment is necessary when repair and maintenance, etc. such as parts replacement was made.
Adjusting method is as explained below. Always adjust or check the +5V power source before adjusting VCO.

2. ADJUSTMENT OF +5V POWER SOURCE (V_{CPU})

1. Connect the AC adaptor connector plug to CN1.
   Check that the output of AC adaptor is approx. 12V.
2. Connect the ⊕ terminal of DC voltmeter to TP1 (D3 cathode side) and ⊖ terminal to GND (power switch fixing angle, etc.) for voltage measurement.
3. Check each part before turning the power SW ON.
   Set VR1 to the center of variable range.
   Connect CN4 with SW. P.W.B. through a flexible cable.
   Connect CN2 with fan motor.
   Disconnect the flexible cable from CN6 to separate it from LCD unit.
   Presence and type of video signal input to CN3 are not specified.
   Check if a conductor is crushed under the P.W.B., or if there is any foreign material mixing.
4. Turn the power SW ON and check that the LED lights up and the fan begins rotating.
5. Rotate VR1 *1 with a ⊖ driver and adjust to approx. 5.1V while checking the voltage on a voltmeter.
6. Turn the power OFF and connect the LCD unit flexible cable to CN6. Wait for 10 seconds and more after turning the power off before connection.
7. Turn the power ON again and make a fine adjustment of VR1 *1 to set the voltage of TP1 to 5.1V ± 0.08V after three-minute of operating.

*1 (Voltage becomes higher by rotating VR1 clockwise ↻, and it becomes lower by rotating it counterclockwise ↺).

3. ADJUSTMENT OF VCO

1. Connect the ⊕ terminal of DC voltmeter to TP5 and the ⊖ terminal to GND (power SW fixing angle), connect the fan motor, LCD unit and SW P.W.B.
2. Input video signal to CN3 according to the timing in the test pattern 1.
3. Turn the power SW ON and operate unit for three minutes.
4. Adjustment of VCO on Low Band side
   Adjust L15 by using a ceramic driver and set the voltage at TP5 to 2.5V ± 0.05V. (*2)
5. Input video signal to CN3 according to the timing in the test pattern 2.
6. Adjustment of VCO on High Band side
   Rotate the core of L14 to adjust the voltage of TP5 to 2.5V ± 0.05V. (*2)

*2 (Voltage of TP5 may vary between when the adjustment driver is contact with the variable core and when it is away depending on the material of adjusting driver to be used. Adjust the voltage to be normal when it is away from the core.)

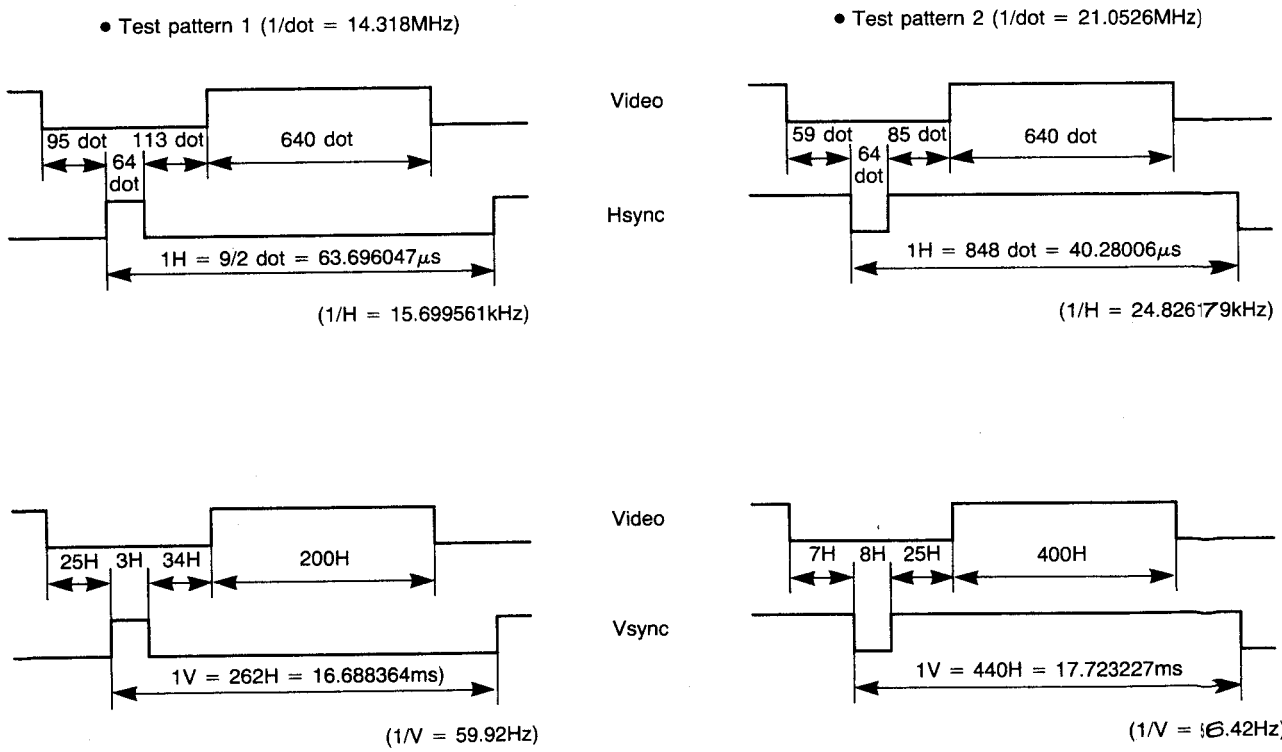


Fig. 1

CIRCUIT DESCRIPTION

1. GENERAL

Circuits will be described in reference to the QA-75 block diagram shown in Fig. 2.

The analog RGB signal from the computer, IBM PS/2 (VGA) or APPLE MAC II, passes through a dedicated cable (optional for APPLE MAC II) and 26-pin input connector, enters the analog input circuit, and converted to a digital RGB signal (R, G, B, SR, SG, and SB).

The digital signal from an IBM-PC EGA or IBM-PC CGA passes through a dedicated cable and 26-pin input connector and enters the digital input circuit.

The input selector selects one of the above as the valid RGB signal and sends it to IC3 in the form R, G, B, SR, SG, and SB.

IC3 decodes the input R, G, B, SR, SG, and SB signals to a 4-bit signal according to a predefined combination. The 4-bit signal is written into the frame memory on ICs 6 and 5.

The writing is controlled by HBL and VBL signals generated from Hsync and Vsync signals. However, for the APPLE MAC II, HBL and VBL signals are generated from Csync signal. (See MAC II synchronizing signal separator.)

PLL (phase-locked loop) circuit, consisting of a phase detector, 1/N divider, LF (loop filter), and VCO (voltage-controlled oscillator), is also used to generate a dot clock from Hsync (Csync for MAC II) signal.

The LCD control is asynchronous from the computer signals.

To improve display quality, the upper and lower halves of the screen are controlled separately.

This is achieved by first writing the RGB data sent from the computer into a frame memory, and then reading this data out according to the LCD control timing requirements in a form suitable for LCD display.

On IC3 timing signals for this purpose are generated in the LCD timing controller, and display data is read out from IC6 and IC5 by controlling field memory read signal generator.

The QA-75 has ENLARGE functions (4 × enlargement, and displaying a 200-line signal in 400-line). These functions are performed with a line buffer (IC8).

To enlarge a display, one horizontal line display data is read out from the field memory and displayed, and also written in the line buffer IC8. Then the data in the line buffer IC8 is read out again and used as the second horizontal display line.

Since the QA-75 has 16-shading display with thinned-out patterns (See Note 1) system, the shading pattern ROM ICs 9 and 7 determine whether dot data that has just read out should be ON or OFF according to the data from the shading information counter.

The LCD display data generator converts the shading data from ICs 9 and 7 to LCD display data DU3-0 and DL3-0.

The QA-75 has a pointer display function. IC4 (M.P.U.) produces pointer position data and the pointer generator generates pointer display. The LCD display data generator adds these data to DU3-0 and DL3-0.

The QA-75 also displays an operation help menu screen. The menu screen generator, IC4 (M.P.U.), generates a menu screen data. That data is written in the menu screen SRAM (IC10), then from which data is read out with a proper timing to build up LCD display data. The LCD display data generator overlaps that data on DU3-0 and DL3-0.

IC4 (M.P.U.) is an 8-bit one-chip microcomputer that controls IC3 via a remote controller and key matrix.

IC4 (M.P.U.) receives divider signals for Hsync and Vsync, and polarity signals from DIVIDER FOR AUTOMATIC SET UP on IC3 and discriminates the signal by its type. It then feeds back appropriate signals to IC3 and select an appropriate VCO according to the type of input signal.

IC4 (M.P.U.) controls the LCD driver voltage (V_{EE}) according to the signal from the contrast key in the key matrix.

IC4 (M.P.U.) generates codes that correspond to the remote controller operations and send them out as serial data through IC11.

As described earlier, IC4 also controls display of the menu screens through IC3.

IC3 contains registers (latches) that hold control values sent from IC4 (M.P.U.). IC4 outputs an address that designates one of these registers. Register values are controlled by outputting data that is input into the register designated by this address.

IC3 is controlled by the values held in these registers.

IC4 (M.P.U.) has an EEPROM. The control data set by the remote controller or key matrix is stored in the EEPROM, which remains when the power is turned off.

(*Note 1) Thinned-out pattern system is a method of implementing shading display by controlling the number of times each dot is displayed in a certain period (several frames).

Because of the operating principle, intermediate shading causes flicker. The flicker becomes serious especially when displaying a relatively large object with a uniform shading.

To reduce flicker, a certain area is thinned out by patterns, instead of simply turning on and off an entire area. Within an area of uniform shading, the period of switching on and off each dot is the same. However, its frame is different, so that an entire area indicates less flicker. This method of reducing flicker is called thinned-out pattern system.

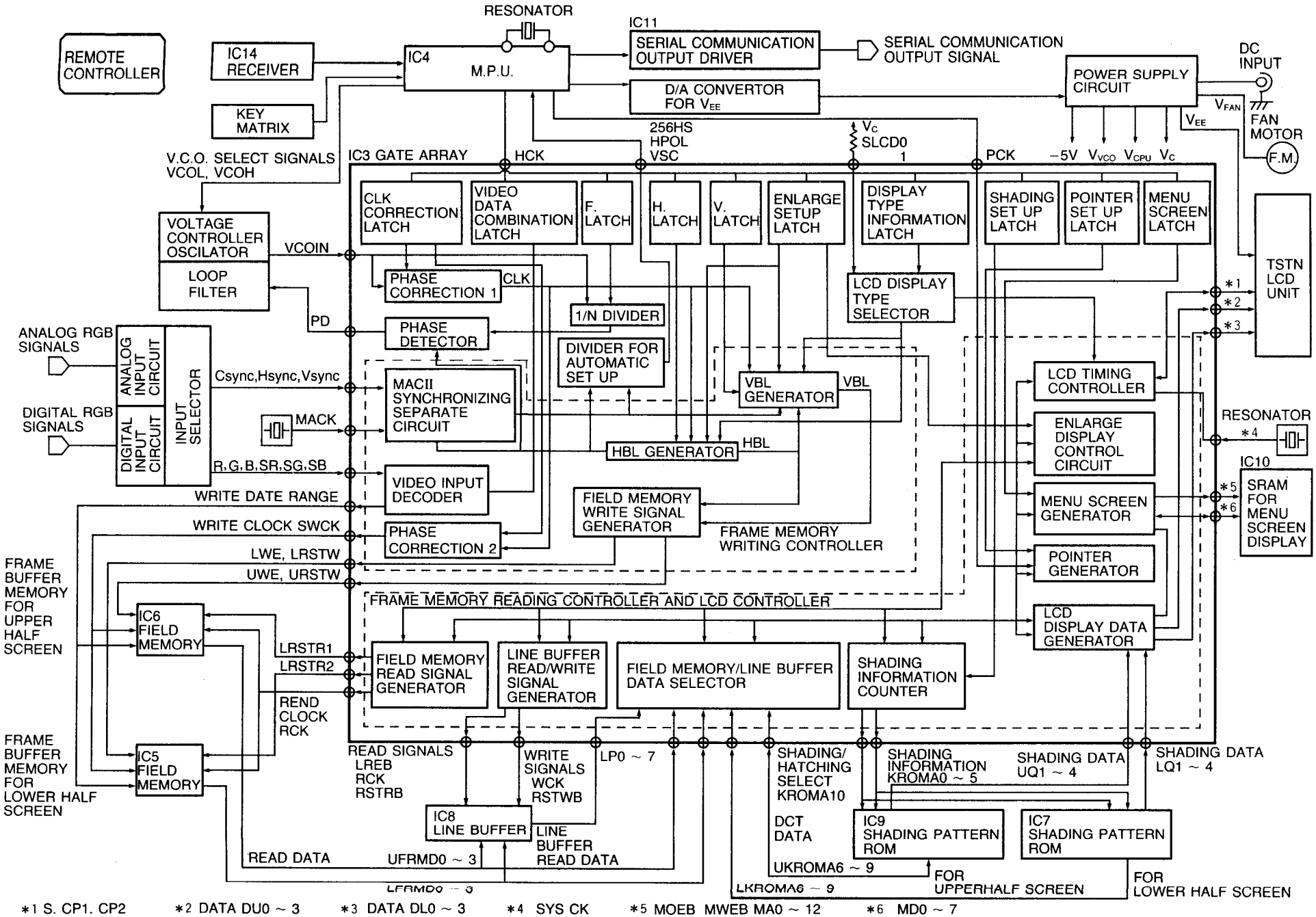


Fig. 2 QA-75 BLOCK DIAGRAM

2. VIDEO SIGNAL INPUT CIRCUITS

The QA-75 accepts either two types of video signals: Analog signals from IBM PS/2 and APPLE MAC II; and digital signals from IBM PC/AT/XT's MDA, CGA, and EGA. These signals are supplied through a 26-pin connector (CN3), then to the analog video input circuit or the digital video input circuit. The following description refers to Fig. 3.

2.1. Digital/analog video signal selection

The video signal is input through connector CN3. Digital video signal passes through AND gates (IC30 and IC31) and enters the B-inputs of the data selector (IC35 and IC36). Analog video signal is processed by analog-to-digital converter built with comparators (IC18 – IC26), then supplied to A-inputs of the data selector (IC35 and IC36). A signal to the data select terminals (pins 1) of IC35 and IC36 selects either A-inputs or B-inputs. This selection signal is input from pin 9 of connector CN3. The signal has the following meaning:

Connecter CN3, pin 9 : OPEN — Digital signal selected (Pins 1 of IC35 and IC36 are high.)
GND — Analog signal selected (Pins 1 of IC35 and IC36 are low.)

2.2. Digital video signal input circuit

The EGA outputs a 6-bit (R, G, B, r, g, b) TTL-level video signal. The CGA outputs a 4-bit (R, G, B, I) TTL-level video signal. The MDA outputs a 2-bit (Mono video, I) TTL-level video signal. Connecter CN3's each pin basically carries the following signal.

Table 2

Video Signal	Connector CN3's Pin Number								
	1	2	3	10	11	12	19	20	24
EGA	g	b	r	G	R	B	Vsync	Hsync	GND
CGA	I	×	×	G	R	B	Vsync	Hsync	GND
MDA	I	Mono video	×	×	×	×	Vsync	Hsync	GND

× : Do not care or N.C.

2.3. Analog video signal input circuit

IBM PS/2 and APPLE MAC II have the following levels of video signal at a 75-Ohm load.

Table 3

		Video Signal	
	R	G	B
IBM PS/2	0.7Vp-p	0.7Vp-p	0.7Vp-p
APPLE MAC II	0.7Vp-p	1.0Vp-p (Synchronization signal overlapped)	0.7Vp-p

Each signal component is converted into a 2-bit digital code according to three threshold levels. The conversion is performed by comparators IC18 to IC26. Reference voltages are supplied to pins 2 of these ICs. The video signal is fed to pin 3 of each comparator. While the signal level is lower than the reference voltage, pin 7 indicates a low level. While the signal level higher than the reference voltage, pin 7 indicates a high level. The following table shows the three threshold levels, which are also adjustable by variable resistor VR2.

Table 4

Threshold Level		0.7Vp-p Video Signal	1.0Vp-p Video Signal
V_ℓ	Range (approx.)	0 ~ 0.24V	0.28 ~ 0.52V
	Typical value (approx.)	0.12V	0.4V
V_m	Range (approx.)	0.24 ~ 0.48V	0.52 ~ 0.76V
	Typical value (approx.)	0.36V	0.64V
V_h	Range (approx.)	0.48 ~ 0.72V	0.76 ~ 1.0V
	Typical value (approx.)	0.6V	0.88V

IC27, IC28, IC29, and IC30 generate three 2-bit signals, (R', r'), (G', g'), and (B', b'), from the digital signals from the comparators, according to the conditions shown in the following table.

Table 5

Conditions	Primary Signal (R', G', B')	Secondary Signal (r', g', b')
$V_i < V_\ell$	0	0
$V_\ell \leqq V_i < V_m$	0	1
$V_m \leqq V_i < V_h$	1	0
$V_h \leqq V_i$	1	1

V_i : Input video signal level

The following table shows the signals that are basically supplied through connector CN3.

Table 6

Video Signal	Pin Number of Connector CN3										
	4	5	6	8	9	13	14	15	19	20	24
IBM PS/2	B	G	R	×	GND	B Return	G Return	R Return	Vsync	Hsync	GND
APPLE MAC II	B	G	R	GND	GND	B Return	G Return	R Return	×	Csync	GND

× : N.C.

To distinguish between IBM PS/2 and APPLE MAC II signals, the following control signal should be supplied to pin 8 of connector CN3.

Connecter CN3, pin 8 : OPEN — IBM PS/2 selected (Pin 11 of IC27 is set high.)
GND — APPLE MAC II selected (Pin 11 of IC27 is set low.)

This control signal is also used to switch the threshold level (1Vp-p or 0.7Vp-p) for converting an analog video signal to a digital form.

2.4. Threshold level generator

The three threshold levels (V_ℓ, V_m, and V_h) for converting an analog video signal into a digital form differ for 0.7Vp-p and 1.0Vp-p signals. Since the APPLE MAC II's G-signal has 1.0Vp-p level, the threshold generator circuitry for this signal is slightly different from the other signals (R and B). The following table shows the relation between the basic threshold levels (V_ℓ, V_m, and V_h) and actual elvels used for the signals (R, G, and B) in IBM PS/2 and APPLE MAC II in Fig. 3.

Table 7

Threshold	IBM PS/2			APPLE MAC II		
	R	G	B	R	G	B
V_ℓ	V_L	V_{LM} ($\fallingdotseq V_L$)	V_L	V_L	V_{LM} ($\fallingdotseq V_L$ + 0.28V)	V_L
V_m	V_M	V_{MM} ($\fallingdotseq V_M$)	V_M	V_M	V_{MM} ($\fallingdotseq V_M$ + 0.28V)	V_M
V_n	V_H	V_{HM} ($\sqrt{}_H$)	V_H	V_H	V_{HM} ($\fallingdotseq V_H$ + 0.28V)	V_H

As Fig. 3 shows, V_L, V_M, V_H, V_{LM}, V_{MM}, and V_{HM} are generated by addition circuits built on operational amplifiers IC33 and IC34 based on reference voltages. The following table shows the reference voltages indicated at the specified points in Fig. 3.

Table 8

	V_0	V_1	V_2	V_3	V_4	V_5
Reference voltage (approx.)	1.23V	0.24V	0.48V	0.24V	0 ~ 0.24V	0.02V (PS/2) 0.28V (MAC II)

V_4 level is adjustable with variable resistor VR2. The actual threshold levels are obtained as follows.

$$\begin{cases} V_L \fallingdotseq V_4 \\ V_M \fallingdotseq V_1 + V_L \\ V_H \fallingdotseq V_2 + V_L \end{cases} \qquad \begin{cases} V_{LM} \fallingdotseq V_5 + V_L \\ V_{MM} \fallingdotseq V_5 + V_M \\ V_{HM} \fallingdotseq V_5 + V_H \end{cases}$$

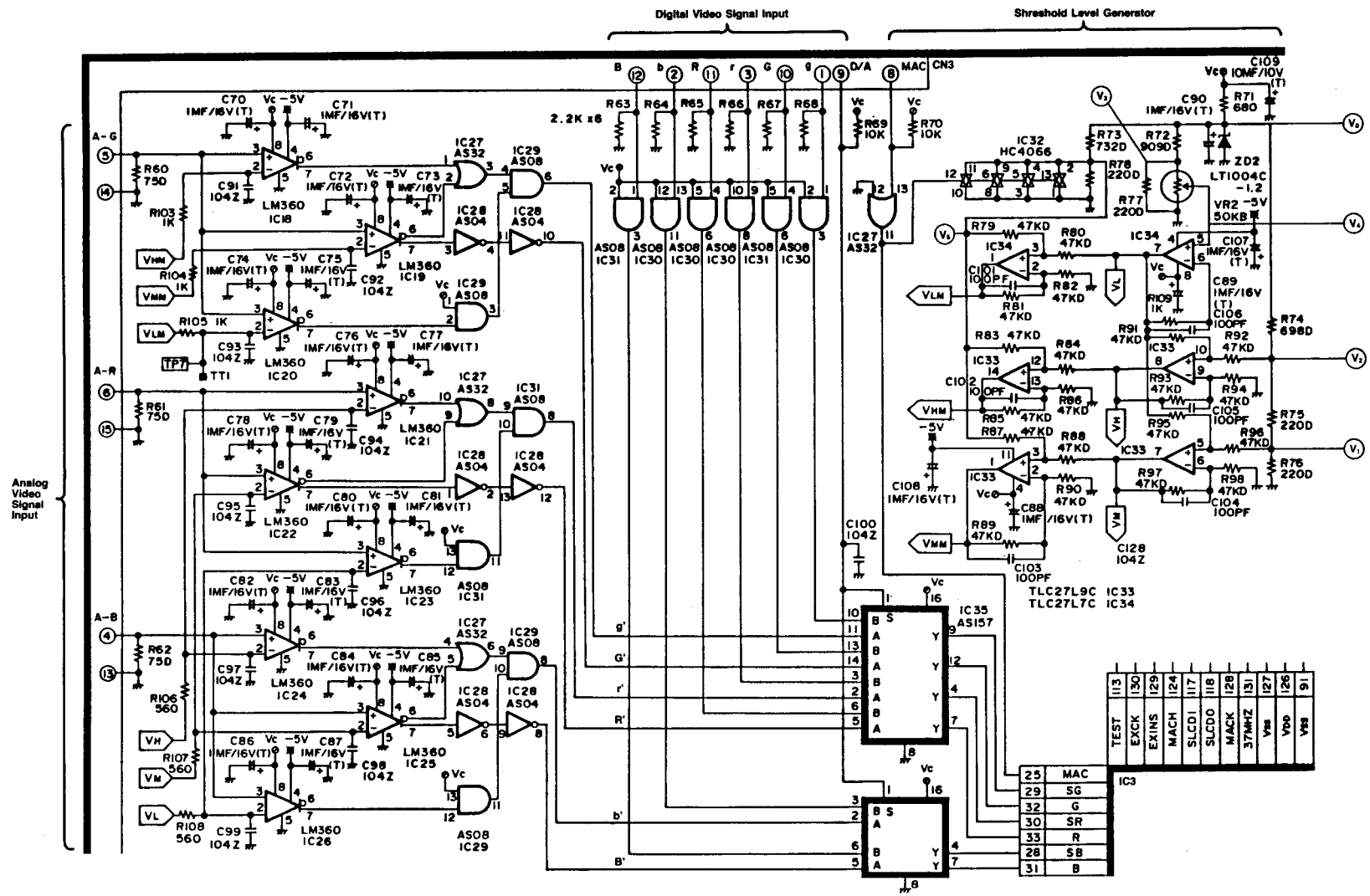


Fig. 3 VIDEO SIGNAL INPUT CIRCUITS

3. PLL CIRCUIT

A dot clock is required to sample a video signal from the computer and extract proper dot data. The dot clock, f_{ck}, is generated by the PLL circuit shown in Fig. 4.

The horizontal sync, f_H, is compared to the feedback signal, f_F, by the phase detector on IC3. If there is a phase or frequency difference in f_H and f_F signals, pin 120 (PDB) of IC3 goes either low or high level. If the phases and frequencies match, the PDB pin goes to high impedance. The output signal from the PDB pin is converted by a loop filter into a d.c. voltage, which controls the VCO.

There are two VCOs, IC15 and IC16 (both are SP1648). IC15 is for high frequency (20.8 to 30.24MHz) oscillation and IC16 is for low frequency (14.3 to 20.8MHz) oscillation. The capacitance of varactor diode (D10 or D11) and the inductance of coil (L14 or L15) determine the oscillating frequency. The voltage applied to the varactor diode is changed to control the oscillating frequency.

One of these VCOs is activated by the signals from pin 58 (VCOH) and pin 57 (VCOL) of IC4.

The control voltage from the loop filter varies the VCO oscillating frequency in the direction that will compensate for the phase difference detected by the phase detector. The VCO output, f_{ck}, passes through IC17 (74HC00), enters pin 123 (VCOIN) of IC3, and has its frequency divided to 1/N by the 1/N variable divider to become feedback signal, f_F. This feedback signal enters the phase detector on IC3 and is compared to the horizontal sync, f_H.

By repeating the above loop, the VCO output, f_{CK}, entering from the VCOIN becomes a dot clock whose phase matches the horizontal sync, f_H and frequency is N times as f_H.

The divider ratio, N, for the 1/N variable divider is controlled by IC4 (M.P.U.) according to the value set in the registers (F-latch). The value can be changed by selecting FREQ MODE in Menu Screen 2.

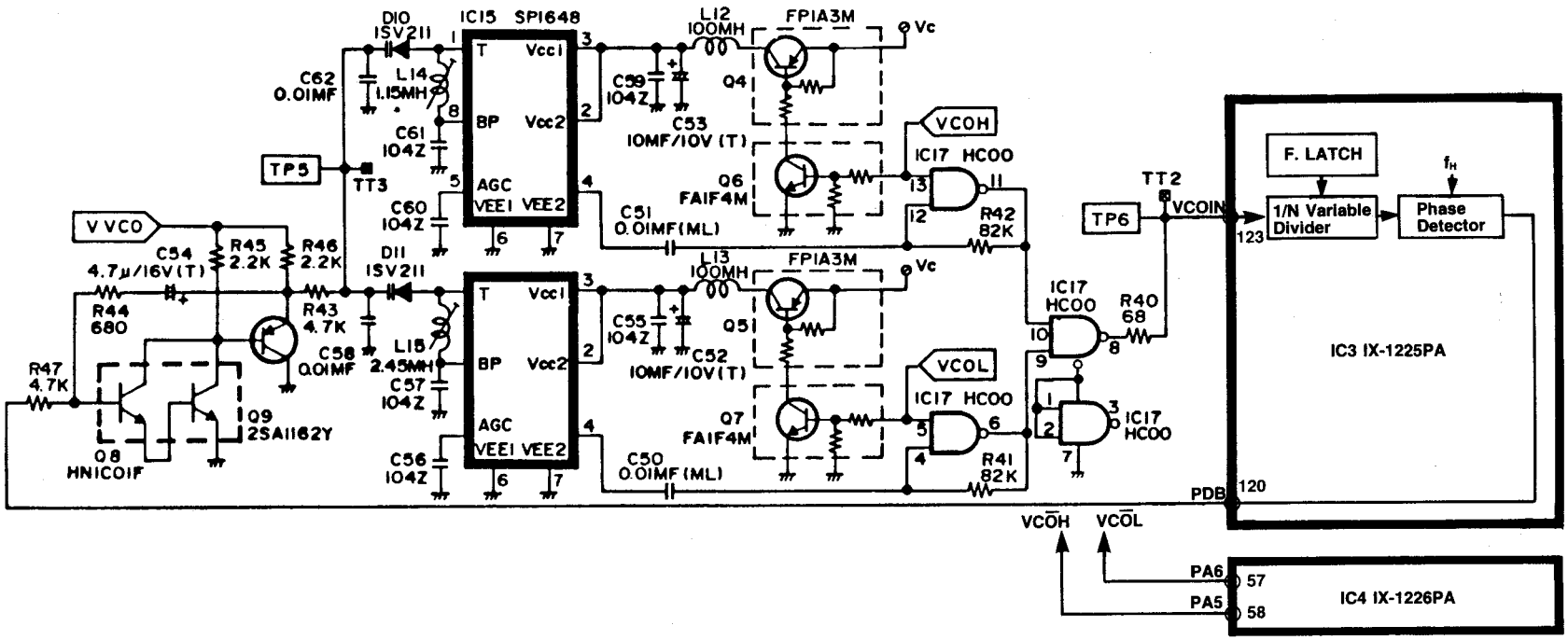


Fig. 4 PLL (Phase-Locked-Loop) CIRCUIT

4. PREPARATION OF HORIZONTAL BLANKING SIGNAL

Horizontal synchronizing signal f_H and video signal have a relation as shown in Fig. 5. Horizontal blanking signal HBL is prepared so that only the data required for display can be selected from the video signals.

The signal preparation circuit consists of an HBL generator and H-latch, as shown in Fig. 2 "BLOCK DIAGRAM."

The period T_{hs}, from the leading edge of horizontal synchronizing signal f_H to the start of the horizontal display period is obtained by dot clock cycle $T_{CK} \times h$. The value of h is set into the registers (H-latch) on IC3.

The H-latch is controlled by IC4 (M.P.U.), and the value of h is equal to H-POS in PANEL's Menu Screen (MENU2), which can be varied by MODE SELECT keys (◁ and ▷).

Corresponding to the varied h-values, display on the LCD moves in horizontal direction. Since the number of horizontal display dots is 640, the horizontal display time will be $640 \times T_{CK}$.

Note: Excessive shifting of horizontal position may cause defective display, such as drifting images.

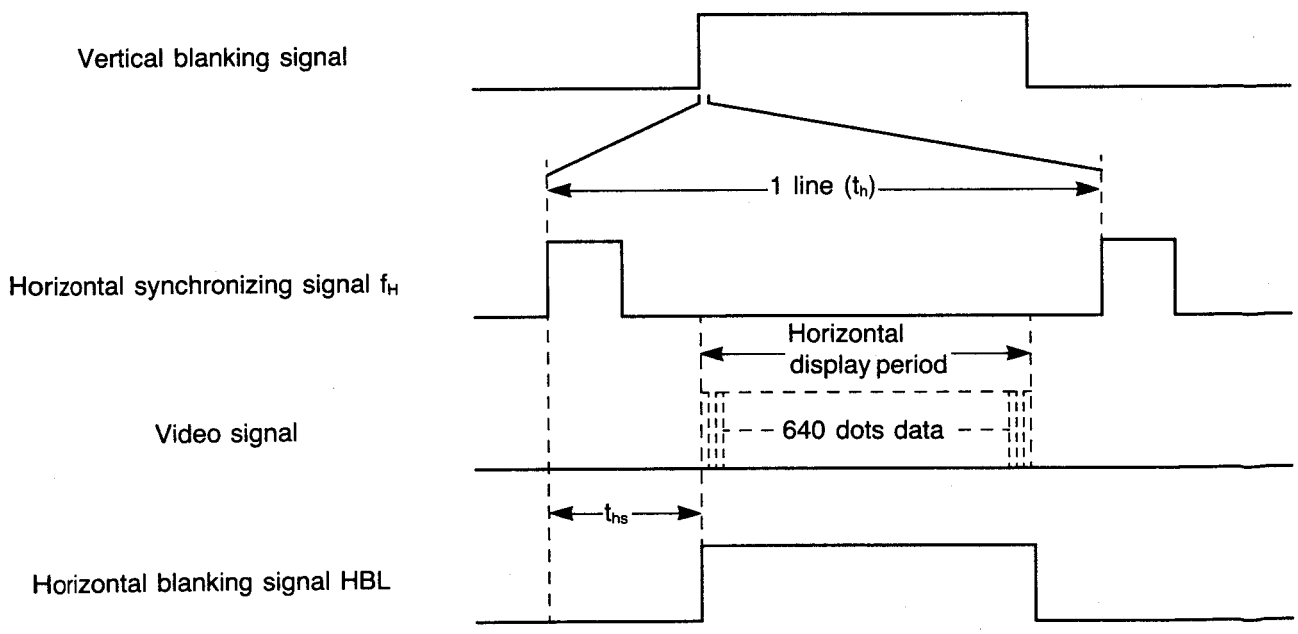


Fig. 5 HORIZONTAL BLANKING SIGNAL

5. PREPARATION OF VERTICAL BLANKING SIGNAL

The relation between vertical synchronizing signal f_V and video signal is as shown in Fig. 6. Preparation of vertical blanking signal VBL is to select only the data effective for display from video signal.

The circuit consists of a VBL generator and register (V-latch), as shown in Fig. 2 "BLOCK DIAGRAM."

The period T_{vs}, from the leading edge of vertical synchronizing signal f_V to the start of the vertical display period is obtained by horizontal cycle $T_h \times v$. This v-value is set into the registers (V-latch) on IC3. The V-latch is controlled by IC4 (M.P.U.), and the value of v is equal to V-POS in PANEL's Menu Screen (MENU2), which can be varied by MODE SELECT keys (◁ and ▷).

Corresponding to the varied v-values, display on the LCD moves in vertical direction.

The vertical display time duration depends on the number of vertical display doets of the video signal being input.

The duration is $480 \times T_h$, $400 \times T_h$, $350 \times T_h$, and $200 \times T_h$, when the number of dots is 480 lines, 400 lines, 350 lines, and 200 lines, respectively.

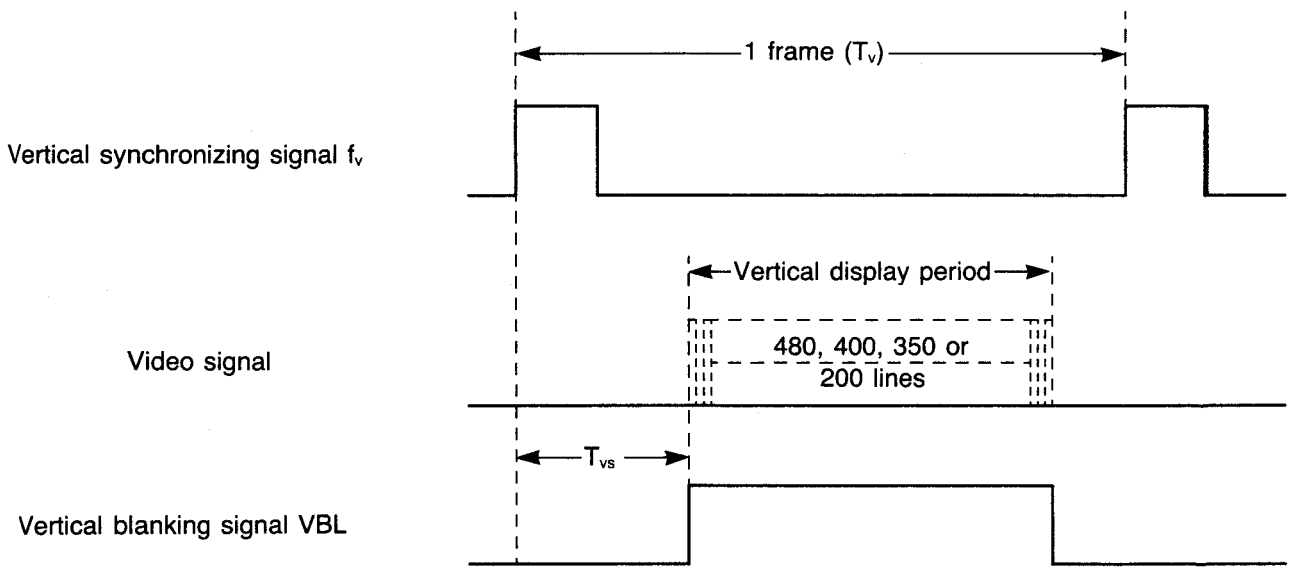


Fig. 6 VERTICAL BLANKING SIGNAL

6. CLOCK AND DATA PHASE COMPENSATION CIRCUIT

Video signals from inputs R, G, B, SR, SG, and SB of IC3 are decoded to 4-bit shading data by the video input decoder on IC3 under the control of IC4 (M.P.U.). Generally, the computer produces video signals and synchronizing signals on the basis of a dot clock, and transmits them to CRT color display. Therefore the dot clock f_{CK}, which is synchronized with the horizontal synchronizing signal, should also be synchronized with the video signal data. However, some of the phases are shifted due to difference of output buffer delay of computer, difference of delay in the input circuit, and distortion of waveform in the signal cables.

To stabilize data from the video signals, the dot clock is delayed so that the relationship shown in Fig. 7 is obtained. Thus, the dot clock signal f_{CK} can sample the centers of the video signal data.

If sampling is made near the boundary between two data, the data value will become unstable. As a result, the LCD will provide flickering displays.

The circuit for the above described function consists of the PHASE CORRECTION 1 circuit and the register (CLK CORRECTION LATCH), as shown in Fig. 2 "BLOCK DIAGRAM."

Delay of the dot clock to video data is controlled by 4 bits out of 5 bits of the CLK CORRECTION LATCH, thus 16 levels of delay time can be made.

Delay time at each level is 2.5ns (TYP). The remaining 1 bit of the CLK CORRECTION LATCH is used for delaying HBL, according to the same reason. The control delays HBL by approximately 15ns (TYP).

A combination of these 5 bits provides 32 levels of phase compensation. For phase compensation control, IC4 (M.P.U.) inputs a control value into the register (CLK CORRECTION LATCH).

The Phase value (0 to 31) on PANEL's Menu Screen corresponds to each of the 32 levels. Thus, using MODE SELECT keys, select the most appropriate level among the 32 levels by checking the display visually, so that non-flickering images can be obtained.

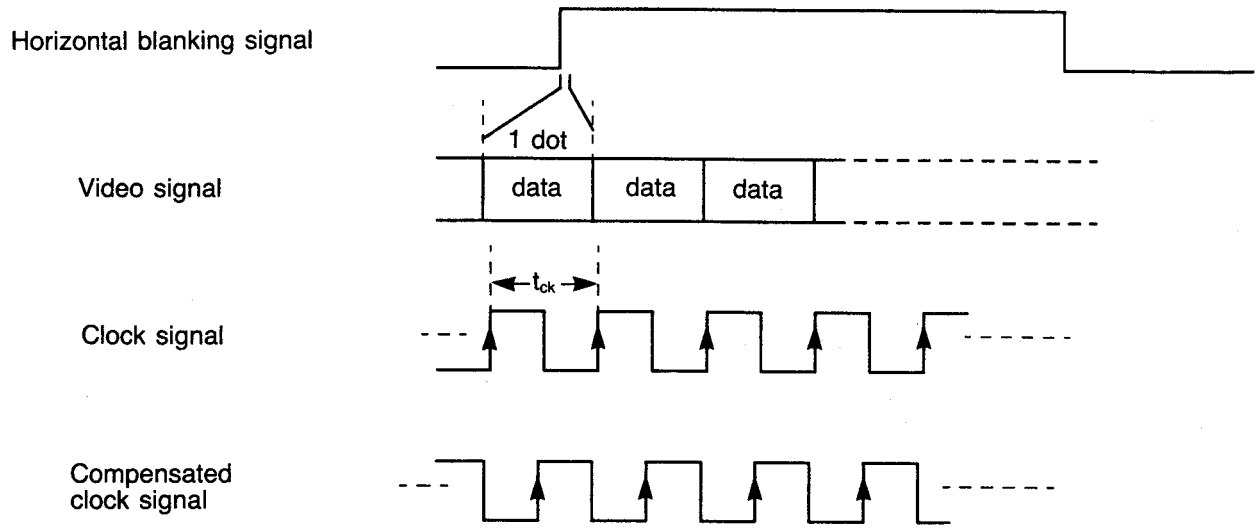


Fig. 7 CLOCK AND VIDEO SIGNAL COMPENSATION

7. LCD CONTROL CIRCUIT

The LCD control signal varies slower than the video signal from the computer. The video signal uses serial data. On the contrary, LCD display data is divided for the upper and lower half screen, each of which is provided with 4-bit parallel data.

To display video signals from the computer on an LCD, the signals for one display must be stored in a memory so that both the upper and lower displays can be read simultaneously on the slow timing for LCD driving.

In Fig. 2 "BLOCK DIAGRAM," a signal for driving the LCD unit is generated on the basis of R, G, B, SR, SG, SB, CLK, HBL, and VBL signals. ICs 6 and 5 are used as a frame memory.

The control circuit consists of a frame memory writing controller, frame memory reading controller, and LCD controller, which are shown in Fig. 2, surrounded by a dotted line. Control signals generated from these circuits control the reading and/or writing of frame memory (ICs 6 and 5), line buffer (IC8), shading pattern ROM (ICs 9 and 7), and menu screen SRAM (IC10), and controls the LCD on the basis of the data from the memory.

Control of each memory will be described from the next page.

8. MEMORY

8.1. Writing field memory

IC3 writes the dot shading data, RAM0 ~ 3 decoded by the video input decoder in the field memory (ICs 6 and 5) using the control signal generated by the field memory write signal generator and write clock, SWCK, which is slightly delayed behind CLK by PHASE CORRECTION 2 (collection value is fixed).

writing operation is performed serially bit-by-bit.

In magnified mode, the upper half of 1/4-screen is written in IC6 and the lower half is written in IC5. The writing operation is performed serially bit-by-bit.

8.2. Reading field memory and writing/reading line buffer

IC3 reads from IC6 (upper screen) and IC5 (lower screen) simultaneously using read clock, SRCK. SRCK is generated by the field memory read signal generator from the SYSCK that is provided through the LCD timing controller. The reading is performed asynchronously from the writing.

In normal mode, the data read from IC6 and IC5 are output to the shading pattern ROMs (ICs 9 and 10) as upper screen dot data (UKROM A6 ~ 9) and lower screen dot data (LKROM A6 ~ 9).

In magnified mode, the two 4-bit data read from the field memory is written in the line-buffer as one 8-bit data, one horizontal line at a time. Then the data for the next one horizontal line (or three horizontal lines for magnified 200-line) is read from the line buffer rather than the field memory. The field memory data/line buffer data selector switches the upper screen dot data (UKROM A6 ~ 9) and lower screen dot data (LKROM A6 ~ 9) so that the data read from the line buffer becomes effective.

The field memory read signal generator and line buffer read/write signal generator control the field memory (ICs 6 and 5) and line buffer (IC8).

8.3. Reading shading pattern ROM

IC3 inputs shading/hatching select (KROMA10) generated by the shading information counter, shading information (KROMA0 ~ 5), upper screen dot data (UKROM A6 ~ 9) and lower screen dot data (LKROM A6 ~ 9) (See the previous section for the last to signals) into the address of shading pattern ROMs, IC9 (upper screen) and IC7 (lower screen). Then IC3 inputs ON/OFF information for each dot, which corresponds to the output from the shading pattern ROMs, into the LCD display data generator on IC3 through UQ1 ~ 4 and LQ1 ~ 4.

8.4. Writing/reading menu screen SRAM

IC4 (M.P.U.) writes the writing address and data that has been latched in a register (menu screen latch) with proper timing.

When the menu screen display is being set, the menu screen generator reads display data from IC10 and converts it to proper LCD display data, which is then overlapped in the LCD display data generator.

9. LCD UNIT

9.1. Interface signal

Table 9

Pin	Signal	Function	Enable Level
1	S	Scan Start-up	H
2	CP1	Input Data Latch	H → L
3	CP2	Data Input Clock	H → L
4	NC		
5	HC		
6	V_{DD}	Power Supply (for Logic)	
7	V_{SS}	GND	
8	V_{EE}	Power Supply (for LCD)	
9	DU0	Display Data for Upper Half	H (ON), L (OFF)
10	DU1		
11	DU2		
12	DU3		
13	DL0	Display Data for Lower Half	H (ON), L (OFF)
14	DL1		
15	DL2		
16	DL3		

9.2. Circuit configuration

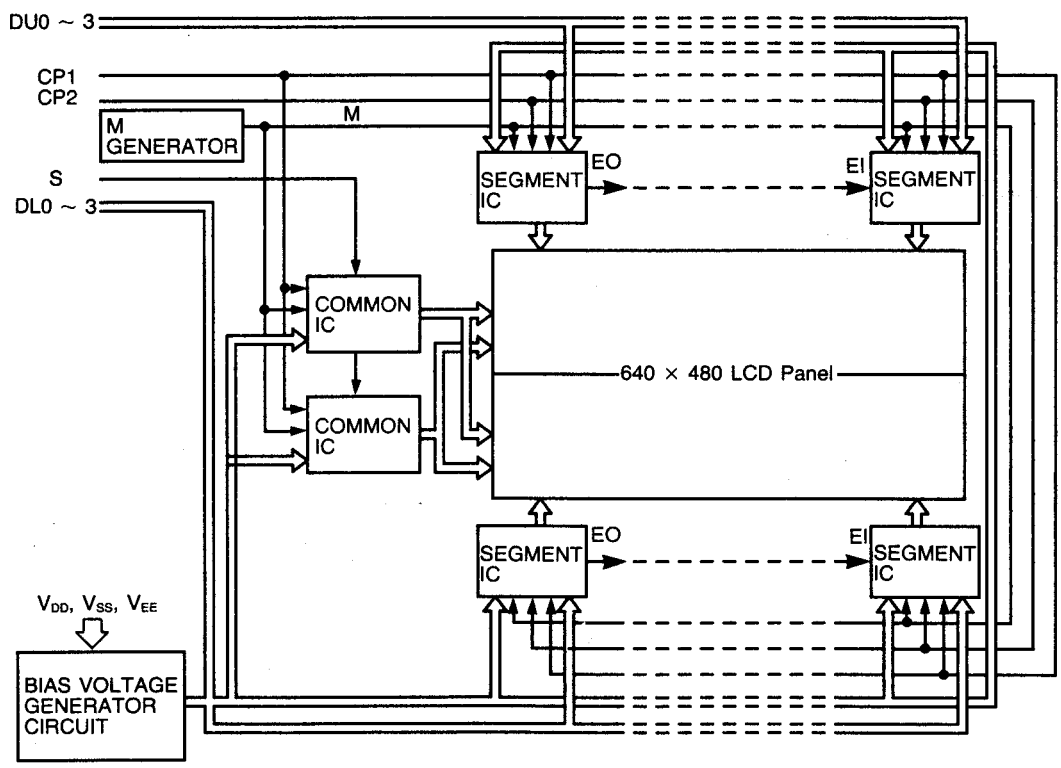


Fig. 8 LCD UNIT CIRCUIT BLOCK DIAGRAM

9.3. Interface signal

Display for the unit is divided into two areas, i.e. upper and lower display segments, for control purposes, so that high contrast images with reduced number of duty can be obtained.

9.4. Input data and control signal

The LCD driver is a 80-bit LSI which consists of a shift register, latch circuit and LCD drive circuit. For both the upper and lower displays, data is input one line by one line (640 dots). Then the data is consecutively transfered from the top left of the display, as 4-bit parallel data, through the shift register, together with the clock pulse CP2.

When 640 dot data (for one line) is input, the latch signal CP1 is turned off to latch the data as parallel data for 640 signal electrodes.

The LCD drive circuit transmits the driving signal S, which corresponds to the 640 signal electrodes of the LCD panel, to the signal electrodes.

At the same time the scanning start signals, which has been sent to the scanning signal driving circuit, are transferred to the first line of the scanning electrode. Thus a combination of the LCD's scanning electrode and the voltage applied to the signal electrodes displays the contents of the signal data on the first line of each display.

While the data for the first line is displayed, data for the second line is input.

When 640 data transfers complete, CP1 is turned off to make a display for the second line.

Thus the data inputting is repeated up to 240th line from the top to the bottom on a time sharing basis. Then the display for one frame completes.

Data inputting restarts frodm the first line. The scanning start signal S is to drive horizontal electrodes.

If a DC voltage is imposed on LCD panel, the liquid crystal in the panel will deteriorate due to a chemical change. Therefore conversion of the driving waveform at the time of every display is required to eliminate the DC voltage.

The driving waveform conversion (to AC) signal M, which is generated in the LCD unit, performs this function.

Power consumption of the LCD unit increases with increasing clock frequency of CP2, which is one of the properties of CMOS driver LSI.

Thus the driver LSI is provided with a 4-bit parallel data transfer system. This system transfers the data through 4 shift registers to reduce the data transfer speed of CP2 clock.

Power consumption of the LCD unit can be minimized by employing this driver LSI.

In this circuit configuration, the 4-bit display data is input through DU0 ~ 3 (for upper half of display) and DL0 ~ 3 (for lower half of display) data input pins. The LCD unit is also provided with a data input bus line system to further decrease power consumption. This system makes each LSI operate

only when appropriate data is transferred.

Data input for the signal electrodes of both the upper and lower displays and chip selection of the driver LSI are as follows;

A driver LSI located at the left end of the display is selected at first. When 80 dot data (20 × CP2) are supplied, the driver LSI on the right side of the first LSI is selected.

The above selection process continues until the data is supplied to the driver LSI at the right end of the display. The process starts simultaneously on both signal electrode drive LSIs for the upper and lower displays.

As described above, data for the upper and lower displays is transferred successively through a 4-bit bus line, from left to right.

The input signal timing is shown in "TIMING CHART (b) LCD CONTROL SIGNALS".

NOTES

1. The LCD units are assembled with special high accuracies. Do not disassemble them.
2. The deflector plates are easy to receive scratches. Handle them with care.
3. Use absorbent cotton or soft cloth softly and carefully to take off stain or dust on LCD panel surfaces. Use filters compressed air to remove dust.
4. If waterdrops are left on the plates for a long time, the LCD panel may be discolored or become blotted. Dub with soft cotton and then use compressed air to blow off dust.
5. The LCD panels are made of glass. Dropping or hitting against hard substances may cause breakdown or cracking of the panels. Treat them with care.
6. The CMOS LSIs used in the LCD units are sensitive to static electricity. Take necessary measures, such as grounding of workers, anti-static mats, grounding wrist-straps.

10. FUNCTIONS OF IC4 (MC68C11A8 M.P.U.)

IC4 is an HCMOS 8-bit single-chip microcomputer. It contains an 8-Kbyte ROM, 512-byte EEPROM, 256-byte RAM, and hardware functions including 8 timers and serial interface and software functions including the instruction of strengthening M6800/M680/system. In the QA-75, IC4 is used to provide the following control functions.

10.1. Controlling of IC3 (LCDC)

IC4 performs the following control functions by operating the registers (latches) on IC3.

a) Setting of display timing parameters
   - Frequency
   - H-position
   - V-position
   - H-polarity
   - Video type
   - Phase

b) Shading/Hatching control

c) Reverse display control

d) Freeze display control

e) Magnified display control

f) Pointer display control

g) Menu screen display

Addressing to the registers and data inputting are executed according to the timing shown in Fig. 9.

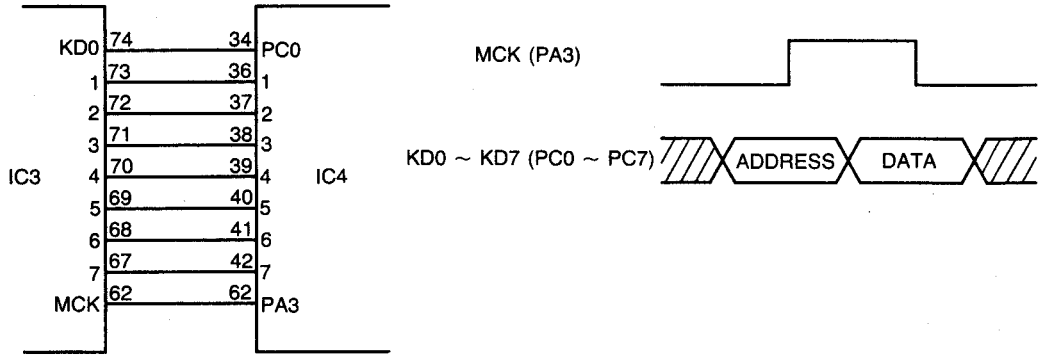


Fig. 9

Gate Array Register (1)

Table 10

Address	Bit	Signal	Description	Remark
01	7	MENU 2	See right table	MENU 2 1 0 / Display State: Menu Area / Message Area 0 0 0: OFF / OFF 0 0 1: OFF / OFF 0 1 0: OFF / Contrast 0 1 1: OFF / Message 1 0 0: Main / Contrast 1 0 1: Main / Message 1 1 0: Remote controller / Contrast 1 1 1: Remote controller / Message
	6	MENU 1		
	5	MENU 0		
	4	WA 12	Menu write address	
	3	WA 11		
	2	WA 10		
	1	WA 9		
	0	WA 8		
02	7	WA 7	Menu write address	
	6	WA 6		
	5	WA 5		
	4	WA 4		
	3	WA 3		
	2	WA 2		
	1	WA 1		
	0	WA 0		
03	7	WD 7	Menu write data	
	6	WD 6		
	5	WD 5		
	4	WD 4		
	3	WD 3		
	2	WD 2		
	1	WD 1		
	0	WD 0		
04	7			
	6		MDA / VGA·EGA / Other	
	5	VGA·EGA	Video process VGA/EGA mode: 0 / 1 / 0	
	4	MDA	Video process MDA mode: 0 / 1 / 1	
	3	S 48	Video band 480 lines	
	2	S 40	Video band 400 lines	
	1	S 35	Video band 350 lines	
	0	S 20	Video band 200 lines	

Gate Array Register (2)

Table 11

Address	Bit	Signal	Description	Remark
05	7	Reserved		
	6	Reserved		
	5	Reserved		
	4	DSL 4	Dot clock phase adjustment	
	3	DSL 3		
	2	DSL 2		
	1	DSL 1		
	0	DSL 0		
06	7			
	6			
	5			
	4			
	3			
	2	FR 10	Dot clock divider ratio	
	1	FR 9		
	0	FR 8		
07	7	FR 7	Dot clock divider ratio	
	6	FR 6		
	5	FR 5		
	4	FR 4		
	3	FR 3		
	2	FR 2		
	1	FR 1		
	0	FR 0		
08	7			
	6			
	5			
	4			
	3			
	2			
	1	HL 9	Horizontal front porch value (H POS)	
	0	HL 8		

Gate Array Register (3)

Table 12

Address	Bit	Signal	Description	Remark
09	7	HL 7	Horizontal front porch value (H POS)	
	6	HL 6		
	5	HL 5		
	4	HL 4		
	3	HL 3		
	2	HL 2		
	1	HL 1		
	0	HL 0		
0A	7			
	6			
	5			
	4			
	3			
	2			
	1			
	0	VL 8	Vertical front porch value (V POS)	
0B	7	VL 7	Vertical front porch value (V POS)	
	6	VL 6		
	5	VL 5		
	4	VL 4		
	3	VL 3		
	2	VL 2		
	1	VL 1		
	0	VL 0		
0C	7			DT 1 / DT 0 / $\overline{K}$ / H: 0 0 16 16A; 0 1 8 16B; 1 0 4 8A; 1 1 2 8B
	6			
	5	K/H	Shading/hatching select 0/1	
	4	DT 1	Shading → Shading level select (2, 4, 8, 16)	
	3	DT 0	Hatching → Hatching pattern select (16A, 16B, 8A, 8B)	
	2	RGB SL 2	RGB select	
	1	RGB SL 1	(Intensity-preference selection)	
	0	RGB SL 0		

Gate Array Register (4)

Table 13

Address	Bit	Signal	Description	Remark
0D	7	SLM	Menu screen Normal/reverse 0/1	
	6	HRV	Horizontal synchronizing signal polarity select	0/1 −/+
	5	Reserved		
	4	SL 4	Normal/reverse display 0/1	
	3	SRGB 3	RGB select (only for hatching mode)	
	2	SRGB 2		
	1	SRGB		
	0	SRGB 0		
0E	7	TEM OFF	Pointer frashing ON/OFF 0/1	
	6	HOME	Pointer home position	When return HOME; 0
	5	Y U/D	Pointer movement direction in Y-direction	Up/down 1/0
	4	X	Pointer movement direction in X-direction	Right/left 1/0
	3	YCRS	Pointer movement direction in Y-direction Enable/disable	Enable/disable 1/0
	2	XCRS	Pointer movement direction in X-direction Enable/disable	Enable/disable 1/0
	1	CRS	Pointer shape select	
	0	CSRON	Pointer ON/OFF 1/0	
0F	7			
	6			
	5	FRZL	Freeze lower screen	
	4	FRZU	Freeze upper screen	
	3	AR 3	Magnified screen select	
	2	AR 2		
	1	AR 1		
	0	AR 0		

10.2. Key data and their functions

Key strobe signals are successively sent from pin 53 (PD4) and pin 54 (PD5) of IC4. Key return data of pin 13 (PE0), pin 15 (PE1), pin 17 (PE2), and pin 19 (PE3) are input to determine which key has been pressed. Internal operation is performed according to the key.

1. MENU key

   It switches ON/OFF Menu Screen 1 or 2.

2. ◁ ITEM SELECT ▷ keys

   They are effective only when Menu Screen 1 or 2 is displayed.

   Each pressing moves an selected ITEM (displayed in reverse) left (or right). Pressing on the leftmost (rightmost) ITEM moves to rightmost (leftmost) ITEM.

3. ◁ MODE SELECT ▷ keys

   They are effective only when Menu Screen 1 or 2 is displayed.

   Each pressing switches the mode of the selected ITEM to previous (next) mode.

4. ◁ CONTRAST ▷ keys

   It increases (or decreases) the LCD contrast control output value (IC4, pin 6 to pin 12 (PB6 to PB0)) by one.

5. Reset key

   It sets each register in IC3 with initial values of timing data for the computer connected. These initial values are also input into IC4 (EEPROM).

10.3. Remote control data and their functions

Data from the remote control signal transmitter is received by light receiver (IC14), and is input into pin 1 (PA0) of IC4. The input data is determined as follows:

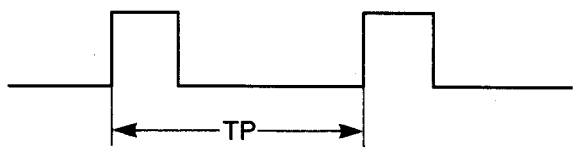


Fig. 10

TP < 0.384ms : Invalid data

0.384ms ≦ TP < 1.664ms : Logic L

1.664ms ≦ TP < 3.392ms : Logic H

3.392ms ≦ TP : Invalid data

The above logic is constructed by 15-bit data, which correspond the code shown in Table 14.

Table 14

INDICATION		REMOTE CONTROL DATA														
MAIN	SUB	C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}
MENU		H	L	L	L	H	L	H	L	L	H	L	L	H	L	X
◁ ITEM SELECT	A	H	L	L	L	H	H	H	L	L	H	L	L	H	L	X
ITEM SELECT ▷	B	H	L	L	L	H	L	L	H	L	H	L	L	H	L	X
◁ MODE SELECT	E	H	L	L	L	H	H	L	H	L	H	L	L	H	L	X
MODE SELECT ▷	F	H	L	L	L	H	L	H	H	L	H	L	L	H	L	X
PC CONTROL		H	L	L	L	H	H	L	L	L	H	L	L	H	L	X
◁ CONTRAST	C	H	L	L	L	H	L	L	L	L	H	L	L	H	L	X
CONTRAST ▷	D	H	L	L	L	H	H	H	H	H	L	L	L	H	L	X
REVERSE	G	H	L	L	L	H	L	H	L	H	L	L	L	H	L	X
CLEAR	H	H	L	L	L	H	L	L	H	H	L	L	L	H	L	X
ENLARGE	I	H	L	L	L	H	H	L	L	H	L	L	L	H	L	X
FREEZE	J	H	L	L	L	H	H	H	L	H	L	L	L	H	L	X
SCREEN	O	H	L	L	L	H	H	H	H	L	H	L	L	H	L	X
POINTER	R	H	L	L	L	H	L	L	L	H	H	L	L	H	L	X
HOME	K	H	L	L	L	H	H	L	H	H	L	L	L	H	L	X
▱ MOVE	L	H	L	L	L	H	H	L	L	H	H	L	L	H	L	X
⬭ MOVE	M	H	L	L	L	H	L	H	L	H	H	L	L	H	L	X
▱ MOVE	N	H	L	L	L	H	H	H	L	H	H	L	L	H	L	X
◇ MOVE	P	H	L	L	L	H	L	L	H	H	H	L	L	H	L	X
◇ MOVE	Q	H	L	L	L	H	H	L	H	H	H	L	L	H	L	X
▱ MOVE	S	H	L	L	L	H	L	H	H	H	H	L	L	H	L	X
⬭ MOVE	T	H	L	L	L	H	H	H	H	H	H	L	L	H	L	X
▱ MOVE	U	H	L	L	L	H	L	L	L	L	L	H	L	H	L	X

C14 is a bit for judging the logic of data as follows:

C14 = L → Data from C5 to C13 are positive logic (positive signal).

C14 = H → Data from C5 to C13 are negative logic (negative signal).

Positive and negative signals are sent alternately at an interval of 6.1ms or longer. IC4 checks these two types of signals to pick up effective signals.

10.4. RESET circuit

IC12 (TL7705CPS-B) detects the power voltage, V_{CPU}, for IC4 and its peripheral parts, and generates $\overline{RESET}$ signal.

If the voltage of V_{CPU} decreases below the detection voltage V_{S1} (TYP 4.5V) when the power is turned off, IC12 shifts the $\overline{RESET}$ signal level to "L."

If the voltage of V_{CPU} increases and exceeds the detection voltage V_{S1} plus hysteresis width V_{HYS1} (TYP 15mV), IC12 starts charging the timing capacitor C152 with a constant current. After the pulse width of t_{po} ($\fallingdotseq 1.3 \times C_t \times 10^4$(s)), C12 shifts the $\overline{RESET}$ signal level to "H."

- Power-off detector

  IC13 (S-8054 ALB) detects the power voltage V_c to generate power-OFF detection signal. If the voltage of V_c decreases below the detection voltage V_{S2} (TYP 4.15V) when the power is turned off, IC13 shifts the power-OFF detection signal level to "L." When the detection voltage of V_c increases and exceeds the detection voltage V_{S2} plus hysteresis width V_{HYS2} (TYP 200mV) when the power is turned on, IC15 shifts the power-OFF detection signal level to "H."

  The power-OFF detection signal is gated at IC39 by the one-shot pulse (generated by IC38 using the leading edge of $\overline{RESET}$ signal as a trigger, t $\fallingdotseq$ 15ms). Thus the signal remains High during the period of the pulse width.

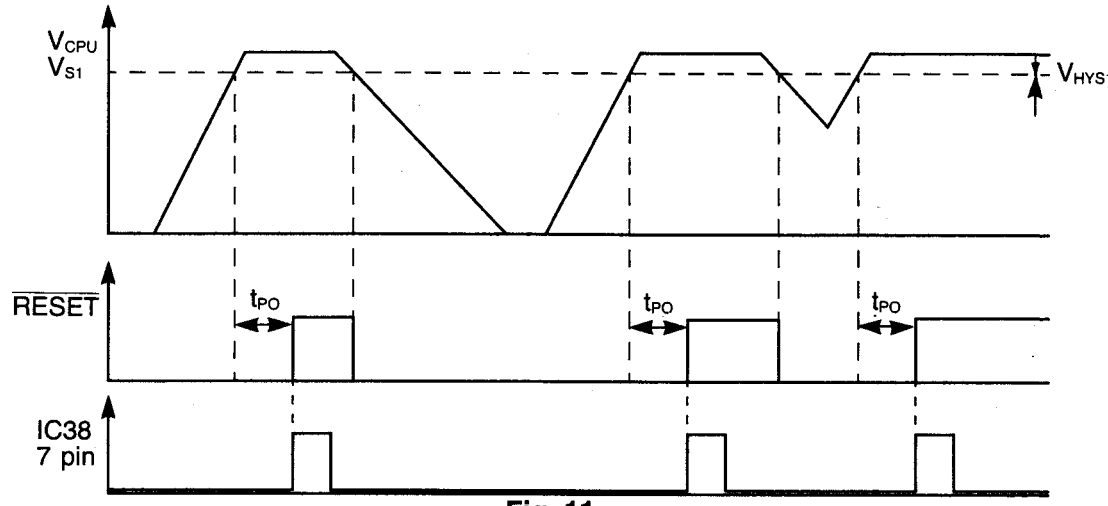


Fig. 11

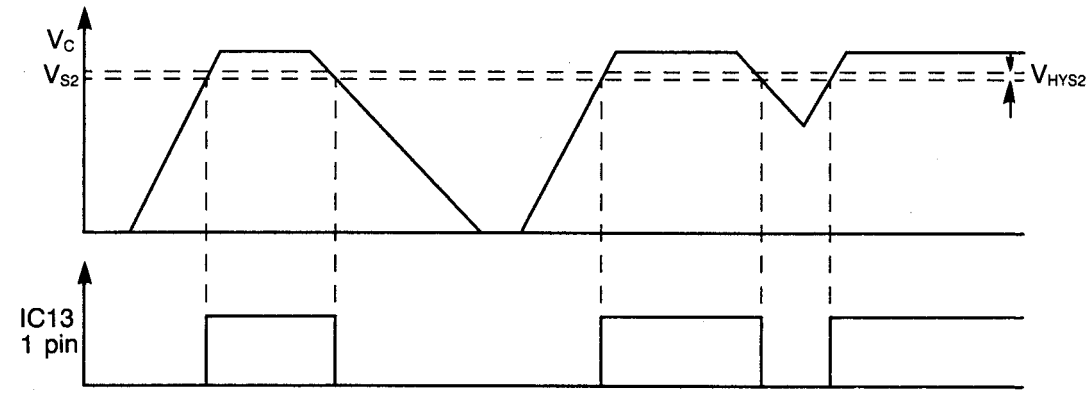


Fig. 12

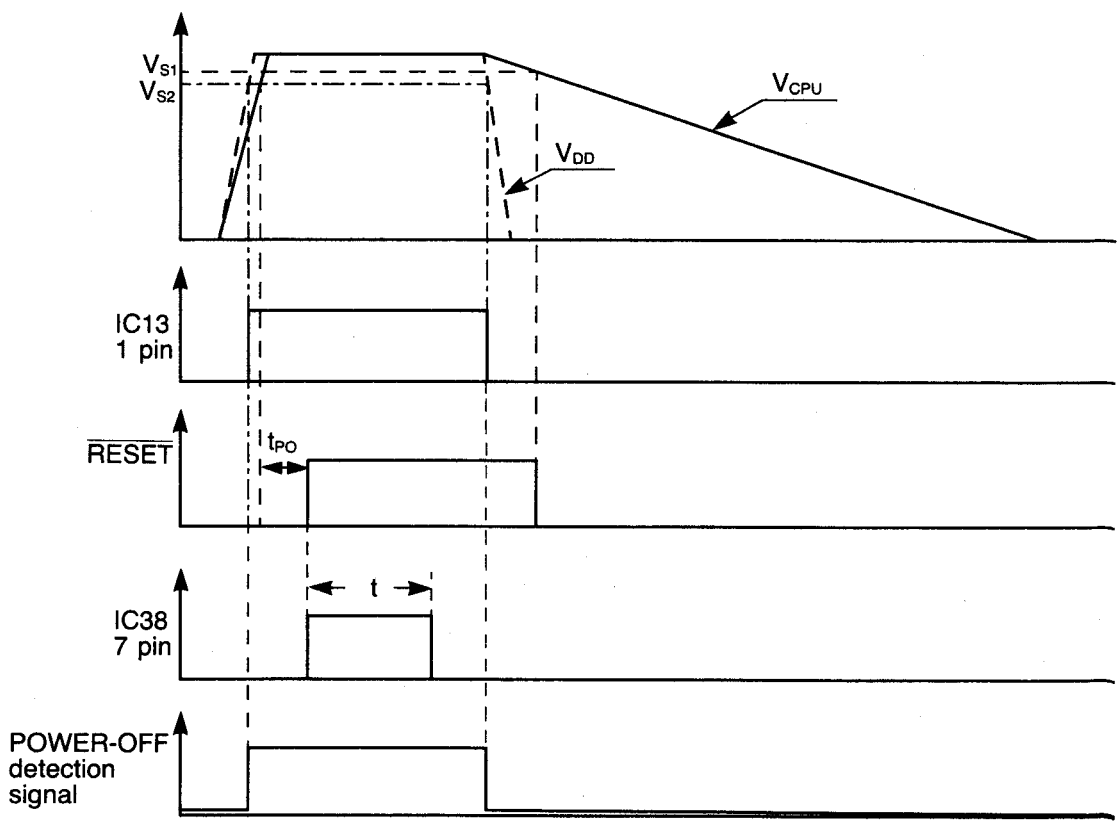


Fig. 13

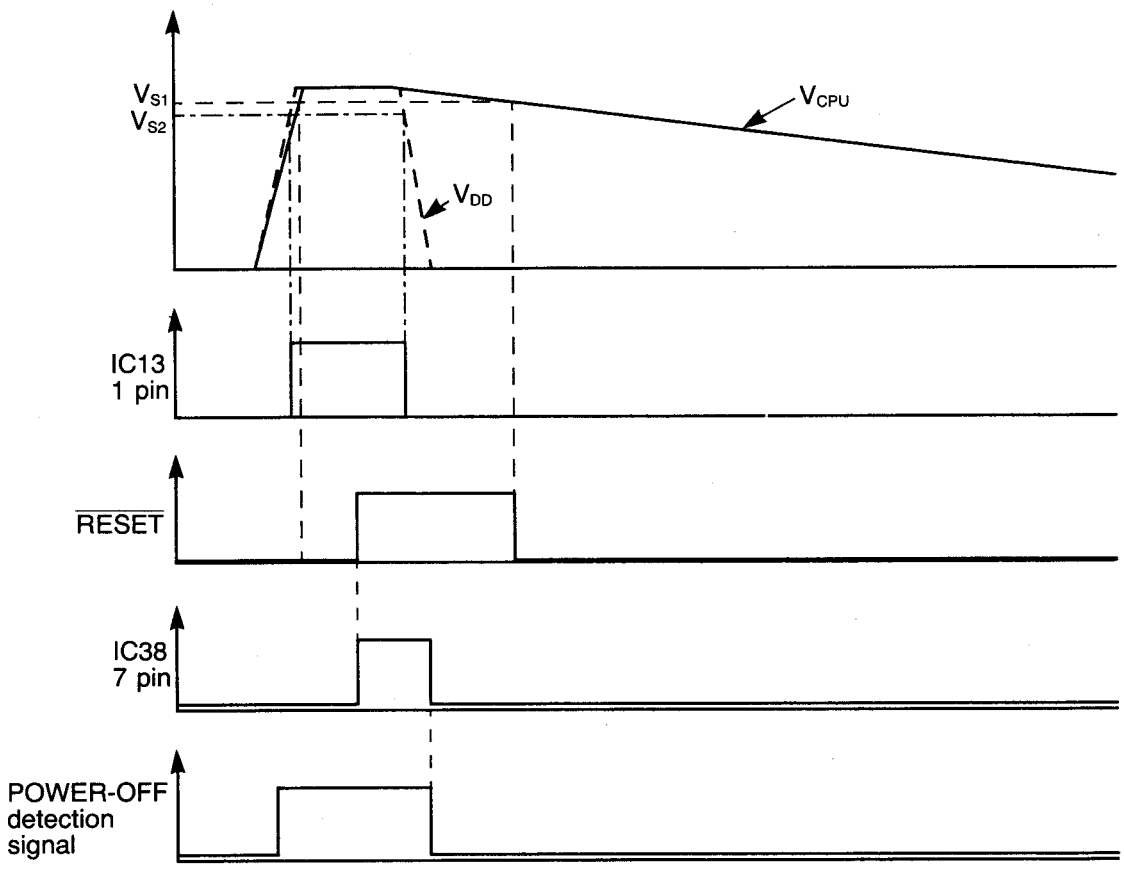


Fig. 14

10.5. Operation of V_c and V_{cpu} and IC4 (M.P.U.)

V_c and $_{cpu}$ increase with the power being turned on. If V_{cpu} exceeds $V_{S1} + V_{HYS1}$, the $\overline{\text{RESET}}$ signal is shifted to "H" level with the timing given in Fig. 11. IC4's reset operation is canceled. The program is executed.

If V_c decreases sharply below V_{S2} when the power is turned off, the power OFF detection signal is shifted to "L." On the other hand, V_{cpu} is backed up by C120 (27mF) capacitor so that it can maintain 4.5V for the time duration of t_w after the trailing edge of the power OFF detection signal. See Fig. 15 (t_w is the time to input the data into EEPROM on IC4.) If V_{cpu} decreases below V_{S1}, the $\overline{\text{RESET}}$ signal level is shifted to "L." Then IC4 starts reset operation.

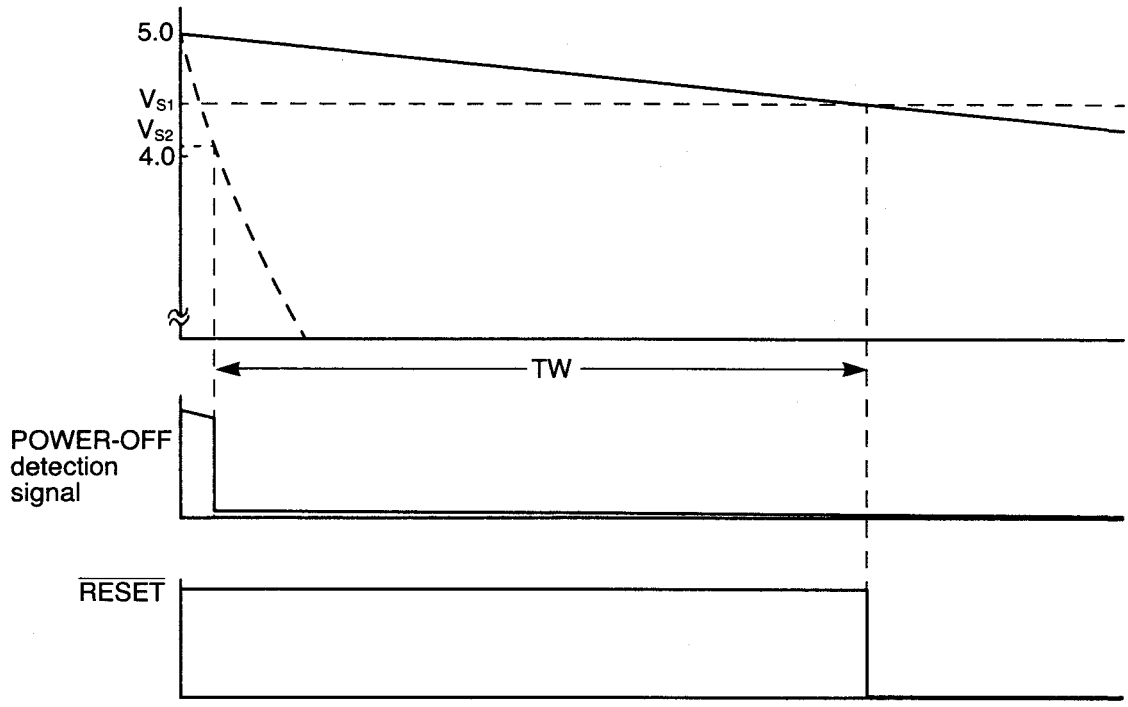


Fig. 15

10.6. Video signal input automatic identification

This function analyzes the video signal from the computer connected to the QA-75, and automatically adjusts input timing.

Automatic identification signals are input from IC3 to IC4.

(1) VSC (IC3, pin 59 → IC4, pin 64)

It is the vertical synchronizing signal of the video signal from the connected computer. IC4 measures the period of this signal.

(2) 256HC (IC3, pin 60 → IC4, pin 63)

It is the horizontal synchronizing signal of the video signal from the connected computer, divided by 256. IC4 measures the period of this signal.

(3) HPOL (IC3, pin 66 → IC4, pin 52)

It indicates the polarity of the horizontal synchronizing signal of the video signal from the connected computer.

H → Positive

L → Negative

IC4 identifies the type of computer from above information (1) PA1 through (3) PA3 according to the identification, IC4 writes the parameters into the registers on IC3 for automatic setting. This function is invalid in the MANUAL set mode.

Signals for selecting one of the VCOs (high band and low band), VCOH and VCOL (positive logic) are transmitted from pin 58 and pin 57 of IC4 respectively.

Identifying of NO CONNECTION:

If 256HC signal remains unchanged for a certain period (approximately 130ms), IC4 identifies NO CONNECTION. It displays "NO CONNECTION" on the LCD, turns both VCOH adn VCOL to "L" level, and stops VCO function.

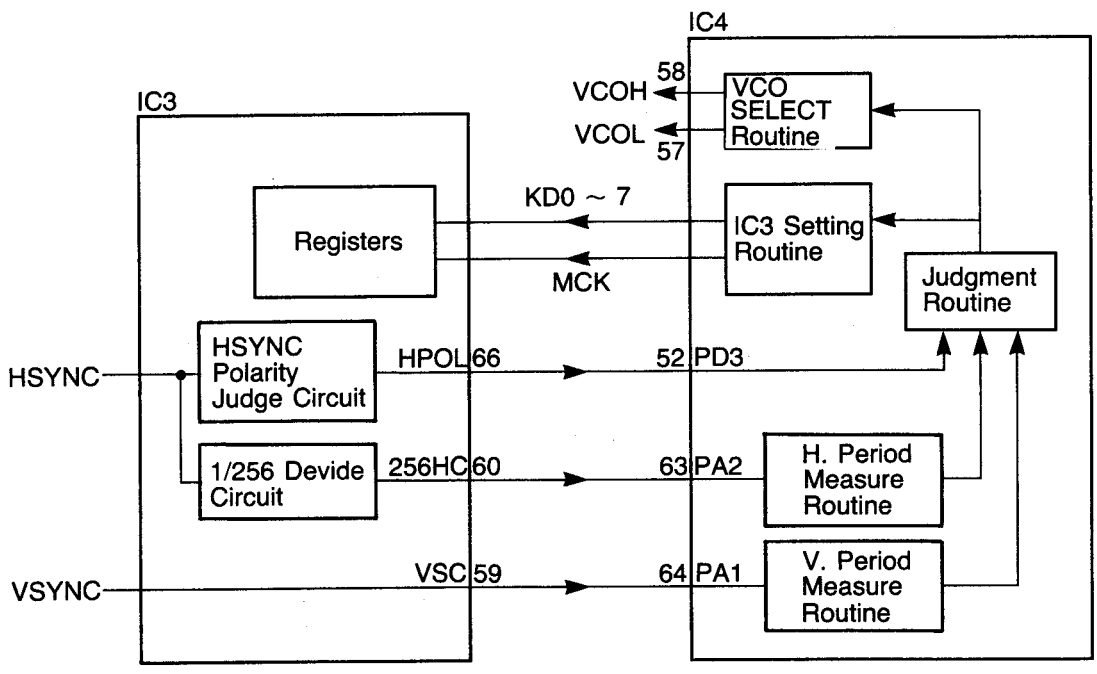


Fig. 16

10.7. Controlling of V_{EE}

The signal for controlling the LCD contrast adjusting negative power is output as a 7-bit (128-steps) signal from pin 6 through pin 12 of IC4 (PB6 to PB0; PB6 is MSB; PB0 is LSB).

$|V_{EE}|$ reaches the minimum for 00H and maximum for 7FH. This value is varied by the contrast ◁ ▷ keys on PANEL or the remote controller.

If CLEAR is turned ON on the Menu Screen 1, or the clear key on the remote controller is pressed, the value is set to 7FH to have the maximum $|V_{EE}|$.

When the RESET key on PANEL is pressed, this value is set to 34H.

10.8. Serial communication circuit

Serial data output signal is output from pin 50 (TXD) of IC4, at CMOS level, in the communication format set in Menu Screen 2. The signal is converted by IC11 (RS-232C driver/receiver) into an RS-232C level signal, then output from CN5. Request to Send and Data Terminal Ready are fixed to +10V.

IC11 contains a charge pump, which enables signal level conversion to ±10V for RS-232C.

The input from the computer (Received DATA, Clear to Send signal, and Data Set Ready signal) are converted by IC11 into a CMOS level signal, and input to IC4. However, the QA-75 does not use Received Data signal.

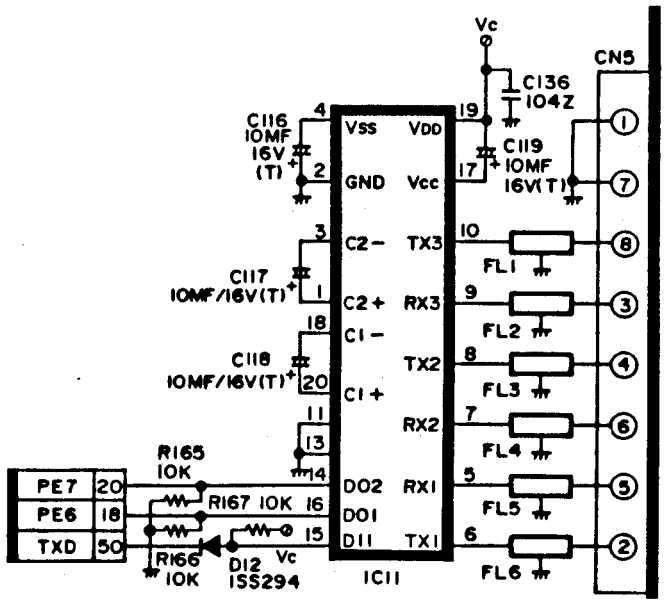
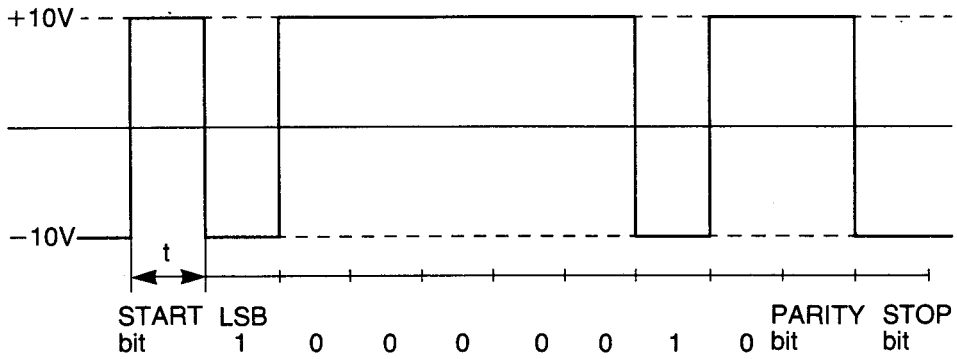


Fig. 17

Example of Serial Signal Output Waveform ("A" code: 41H, data length: 8-bit, parity: EVEN, stop bit: 1-bit)



Baud Rate	t (μsec)
300	3333
1200	833
2400	417
4800	208
9600	104

Fig. 18

10.9. EEPROM control function

IC4 has areas for writing parameters in separate EEPROMs for the computer that can be connected to QA-75. When the power is turned off or video signal is switched, the setting data is retained. When the reset switch is activated, the default values in IC4's mask ROM are written in the EEPROM.

11. POWER SUPPLY

The AC adapter that comes with the QA-75 supplies a fegulated power voltage V_{IN} (12VDC) to the QA-75. From V_{IN}, 5V power (V_{cpu} and V_c), −5V power, LCD contrast power (V_{EE}), and PLL power (V_{VCO}) are made.

11.1. DC-DC converter for +5V (V_{cpu} and V_c)

IC1 in Fig. 11-1 is a controller for a fixed frequency pulse width modulation switching regulator. It contains two controller circuits for different constant voltages.

One of these controllers is used to create 5V power supply from the input power supply V_{IN} (12VDC). (The other controller is used for −5V.)

IC1 contains a saw-tooth wave oscillator whose oscillating frequency is determined by capacitor C21 connected to pin 1 and resistor R18 connected to pin 2. In this circuit configuration, a saw-tooth wave of approximately 75kHz is observed at pin 1 of IC1. Basically this saw-tooth wave is compared to a control signal (observed at pin 5 of IC1). While the saw-tooth wave voltage is smaller than the control signal voltage, the output transistor on IC1 is conductive. The output pulse (indicating the conductive state) is output from pin 7 of IC1 and supplied to the base of the external transistor Q1. The pulse controls the collector cuttent of Q1. The output voltage is fed back to pin 3 of IC1 through R22, R23, and VR1. A reference voltage of 2.5V is output from pin 16 of IC1. On IC1, the half voltage of the reference voltage and the feedback signal supplied to pin 3 of IC1 make the control signal (observed at pin 5 of IC1). As described above, output voltage is stabilized by the pulse width from pin 7 whitch is generated by comparing the control signal with the saw-tooth wave.

The +5V power supply output voltage is adjusted by VR1 so that voltage V_{cpu} at point TP1 becomes 5.1V. Voltage V_c at point TP2 approximately 5V, which is slightly lower than V_{cpu}. This is because the load on the board for V_c is greater than the load for V_{cpu}, so that the forward voltage for diodes D4, D5, and D6 is higher than that for D3.

The voltage supplied to pin 6 of IC1 is called a dead time control signal. It controls the maximum ON period of the output transistor on IC1.

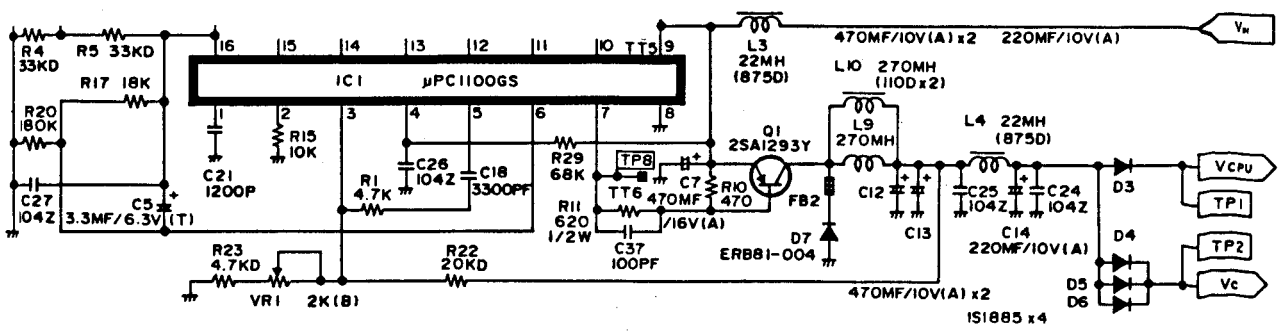


Fig. 19 DC-DC CONVERTER FOR +5V (V_{cpu} and V_c)

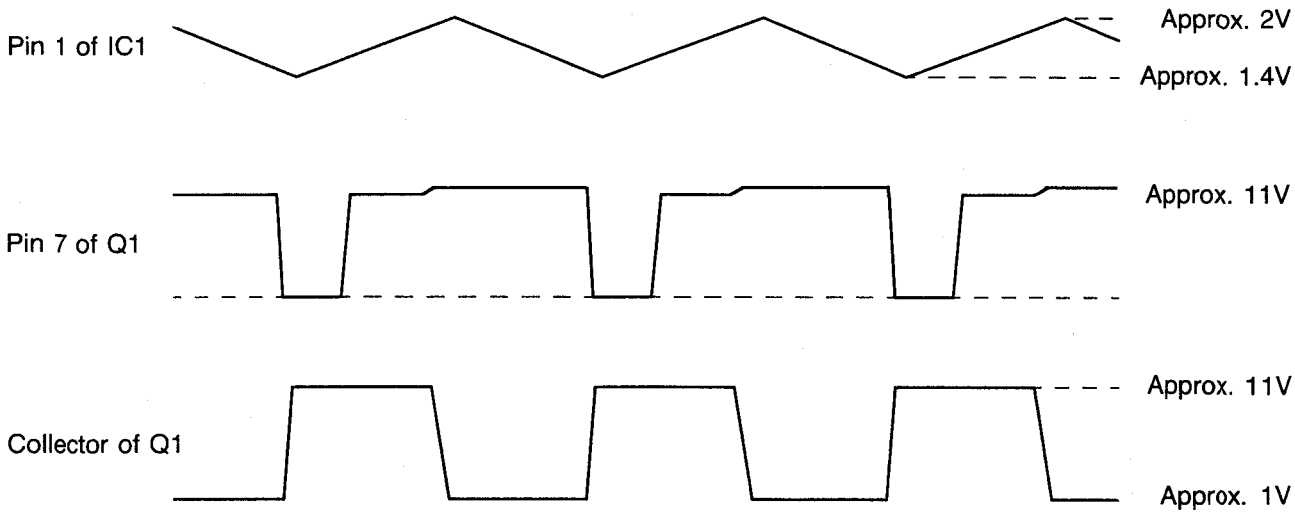


Fig. 20

11.2. DC-DC converter for +5V

One of the constant voltage controllers in the switching regulator controller (IC1) in Fig. 21 is used to configure a DC-DC converter that converts the input power supply V_{IN} (12VDC) to −5V. (The other controller is used for the +5V power supply.)

The same saw-tooth wave oscillator on IC1 for the +5V control is also used for −5V. The basic circuit operation is similar to the DC-DC convertor for +5V.

The output voltage is fed back to pin 13 of IC1. The half voltage of the reference voltage input from pin 14 of IC1 and the feedback signal make a control signal. The control output pulse is output from pin 10 of IC1 and supplied to the base of the external transistor Q2.

−5V should be observed at point TP3 without any adjustment.

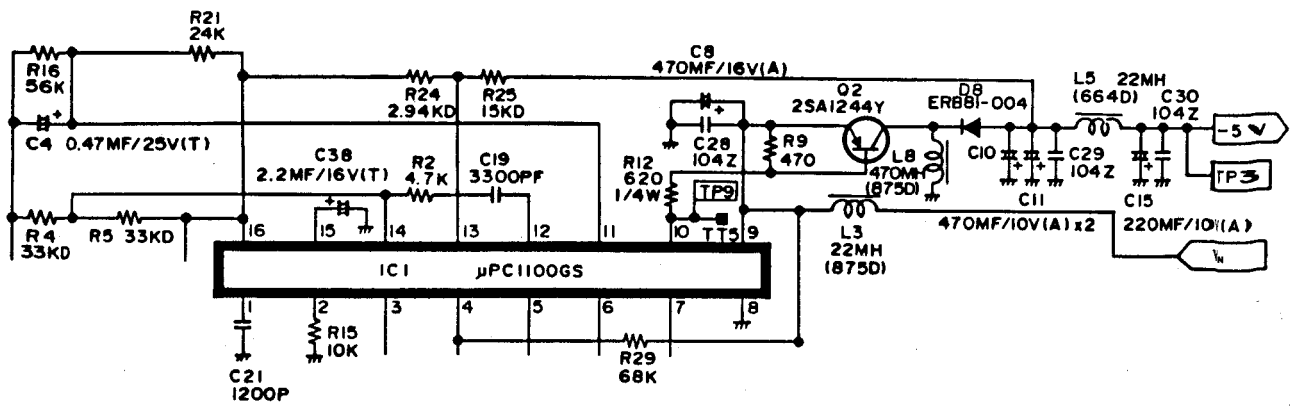


Fig. 21 DC-DC CONVERTER FOR −5V

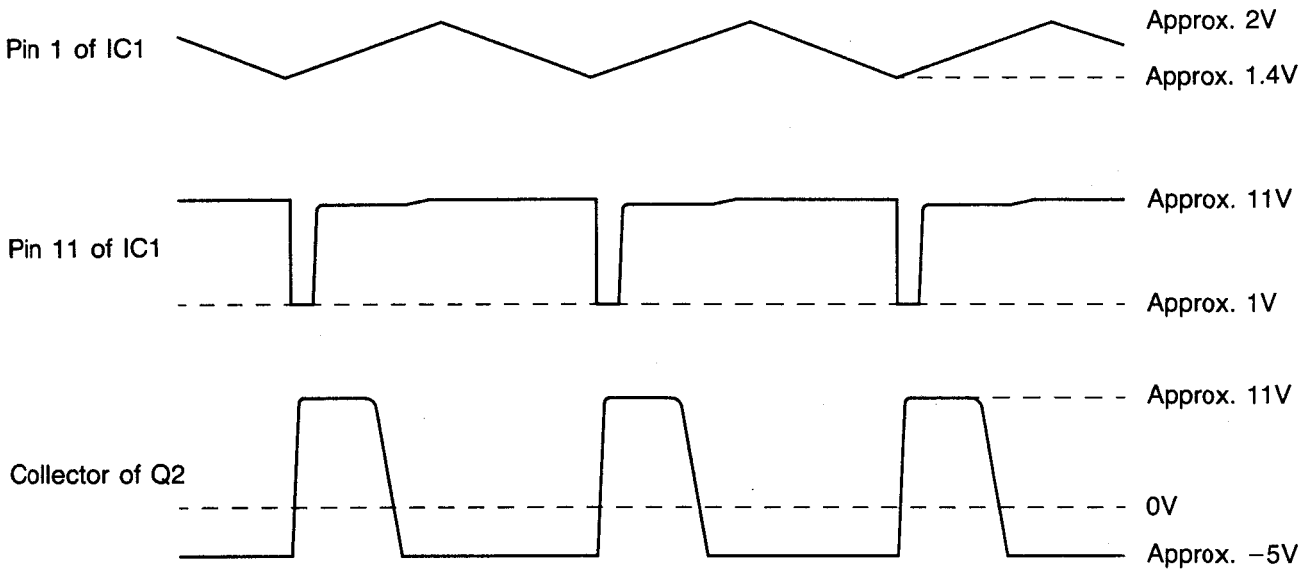


Fig. 22

11.3. DC-DC converter for V_{EE}

Fig. 23 shows the DC-DC converter for generating LCD contrast power supply (V_{EE}). The switching regulator controller, IC2, which is the same IC as IC1, generates negative power supply (V_{EE}) from the input power supply V_{IN} (12VDC).

The oscillating frequency of the internal saw-tooth wave oscillator is determined by capacitor C22 and resistor R14. It is approx. 30kHz and can be observed at pin 1. The circuit has a basic principle of operation identical to the DC-DC converter for +5V.

Feedback signal for output voltage control is produced by circuit comprising of R26, R27, R28, and ZD2, and the circuit comprising of diode arrays DA7, DA8, and DA9, resistors R147, R149, R150, R151, R153, R154, and R155 that are connected to the PB port terminals (pins 6 to 12 of IC4). The feedback signal is controlled so that the voltages of pin 13 and pin 14 of IC2 becomes the same. Resistors R26, R147, R149, R150, R151, R153, R154 and R155, and diodes DA7, DA8, and DA9 construct a current addition type D-A converter. The output voltage (V_{EE}) is controlled by the current of R27 and R28, which is equal to the total of the R26's current and the current from the resistors connected to the 7-bit PB port of IC4. Thus by changing the combination of ONs and OFFs of the 7 bits from IC4, the output voltage (V_{EE}) is varied.

The adjustable range of V_{EE} is approx. −11 to −20V. ZD2 limits the maximum value of V_{EE} to approx. 20V.

The control signal ($V_{EE\text{-}CTL}$) supplied to pin 4 of IC2 controls the output voltage (V_{EE}). When $V_{EE\text{-}CTL}$ is approx. 1V or higher, the output is turned on. The control signal ($V_{EE\text{-}CTL}$) is also controlled by the +5V (V_c). Thus V_{EE} is output only after V_c has reached a valid voltage.

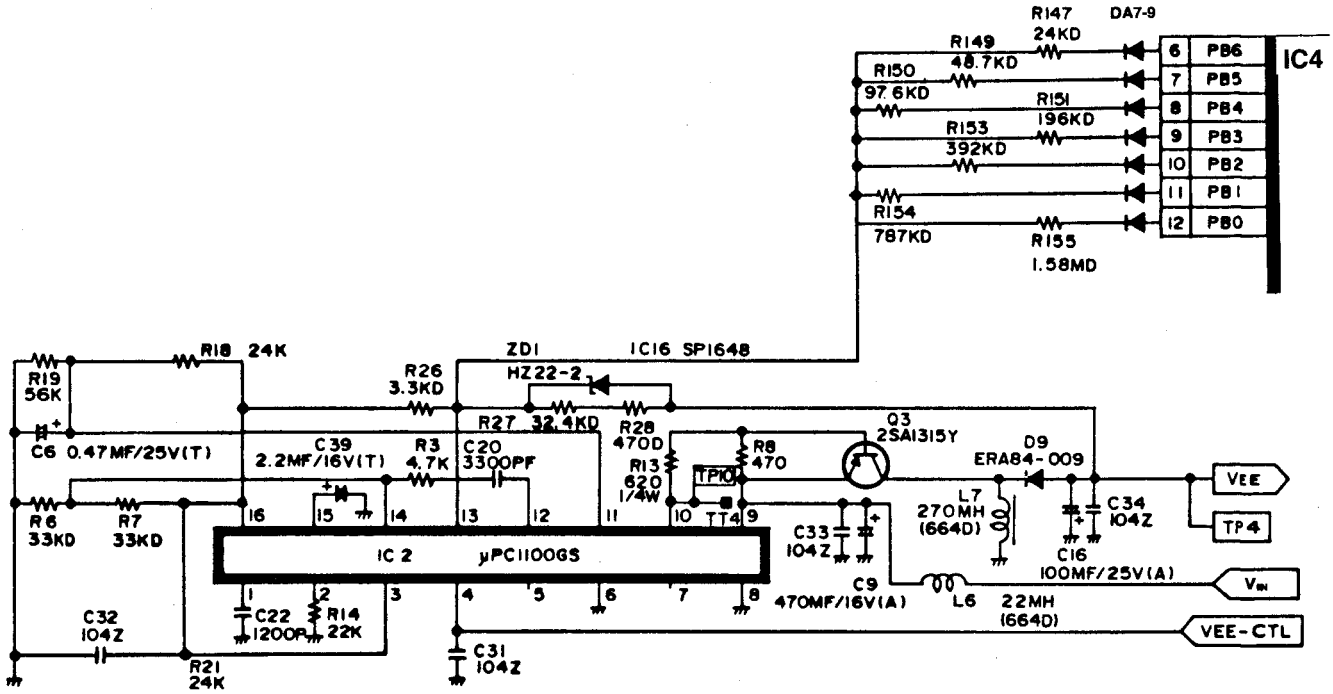


Fig. 23 DC-DC CONVERTER FOR V_{EE}

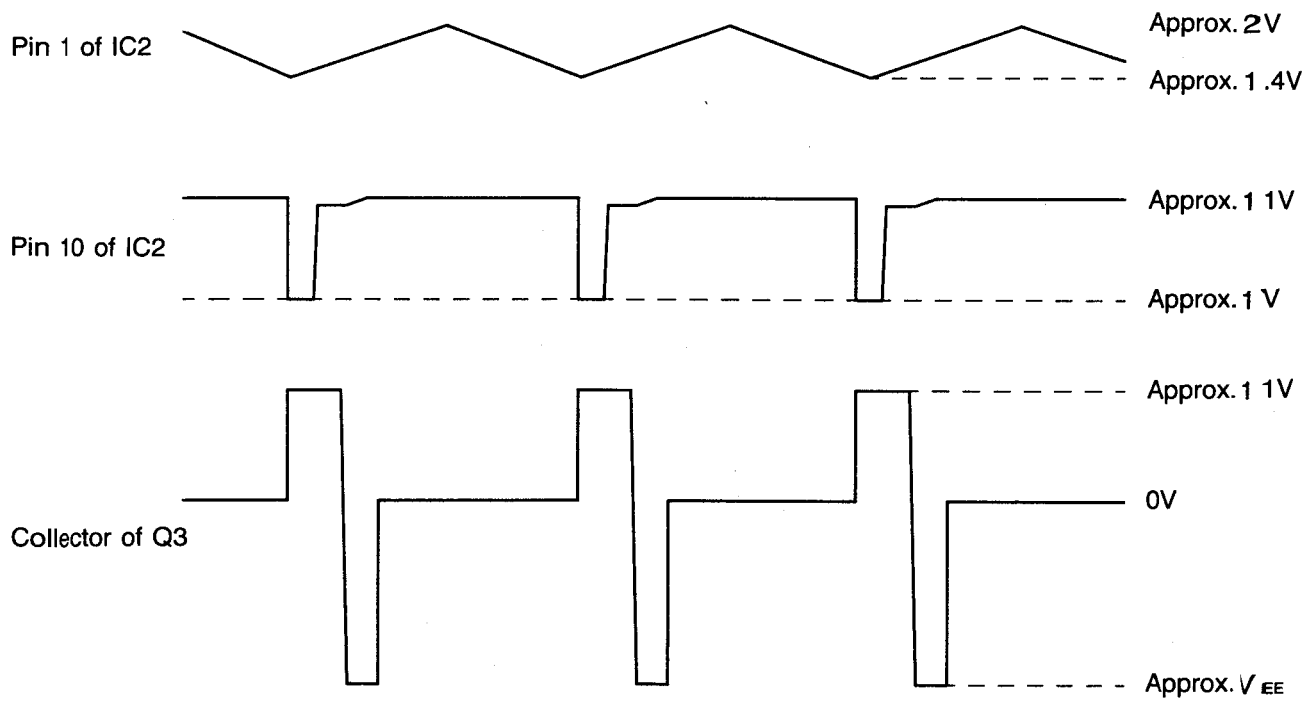


Fig. 24

11.4. Power supply for PLL

Fig. 25 shows the power supply for the PLL, V_{VCO}. V_{VCO} of +10V is generated by a series regulator (IC37) from the input power supply V_{IN} (12VDC).

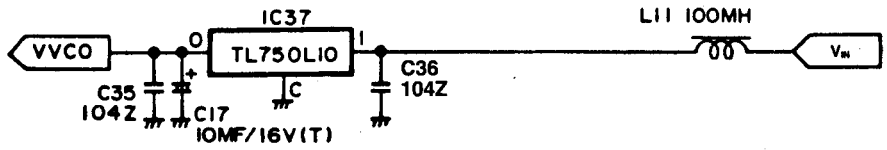


Fig. 25

11.5. Power supply for V_{FAN}

Fig. 26 shows the power supply for the fan motor, V_{FAN}. V_{FAN} is directly obtained from the input power supply V_{IN} (12VDC) through L2.

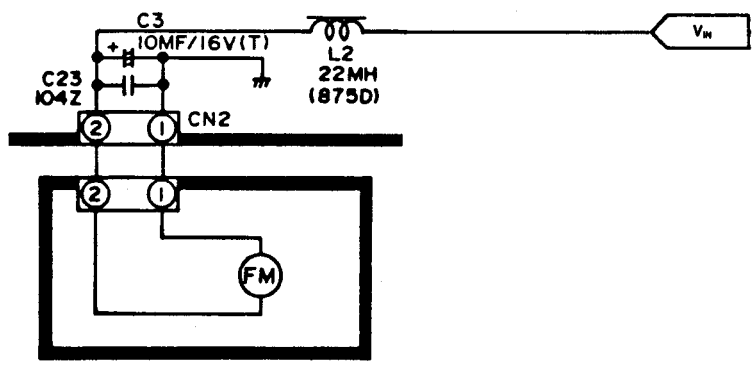
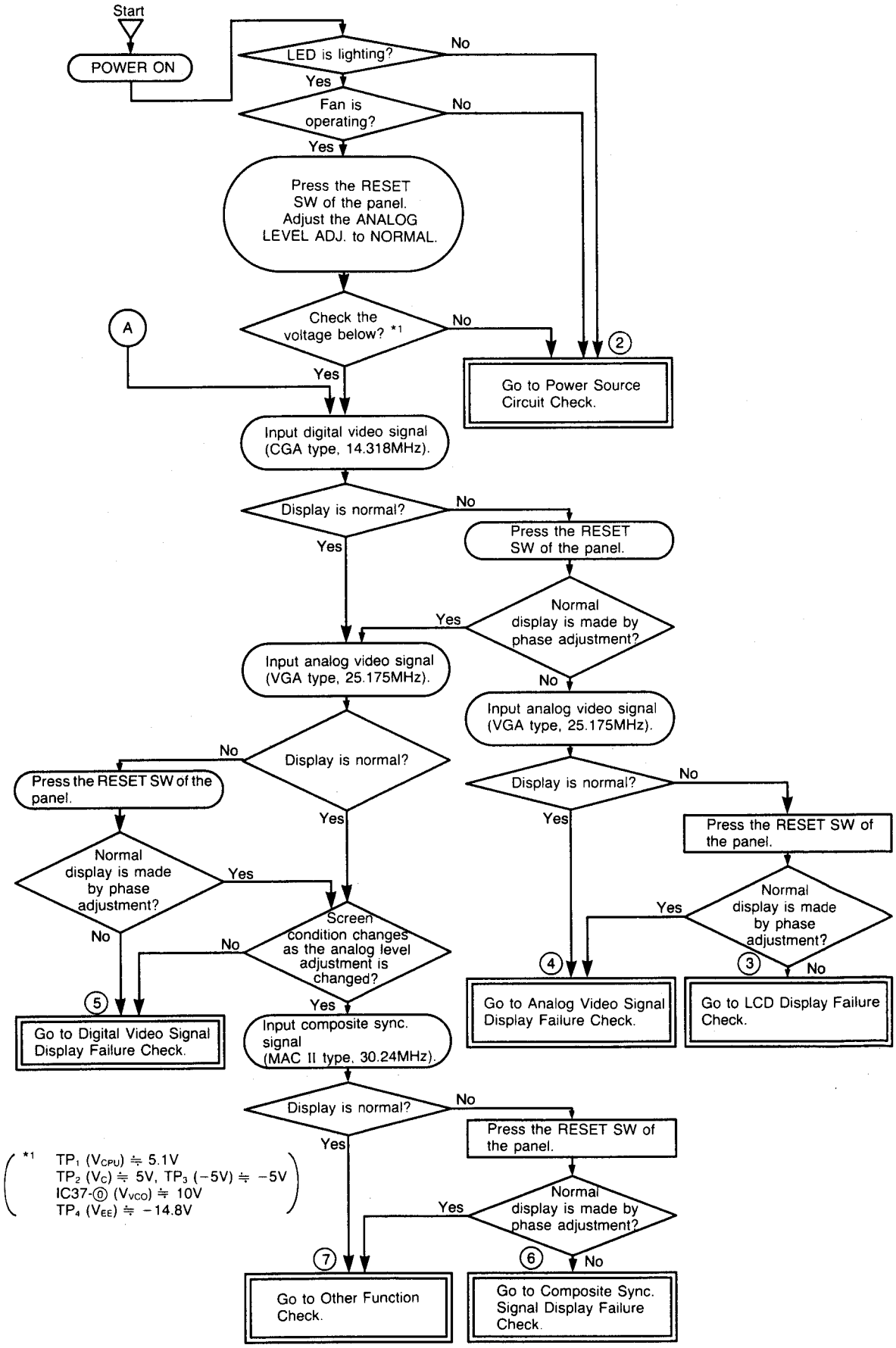
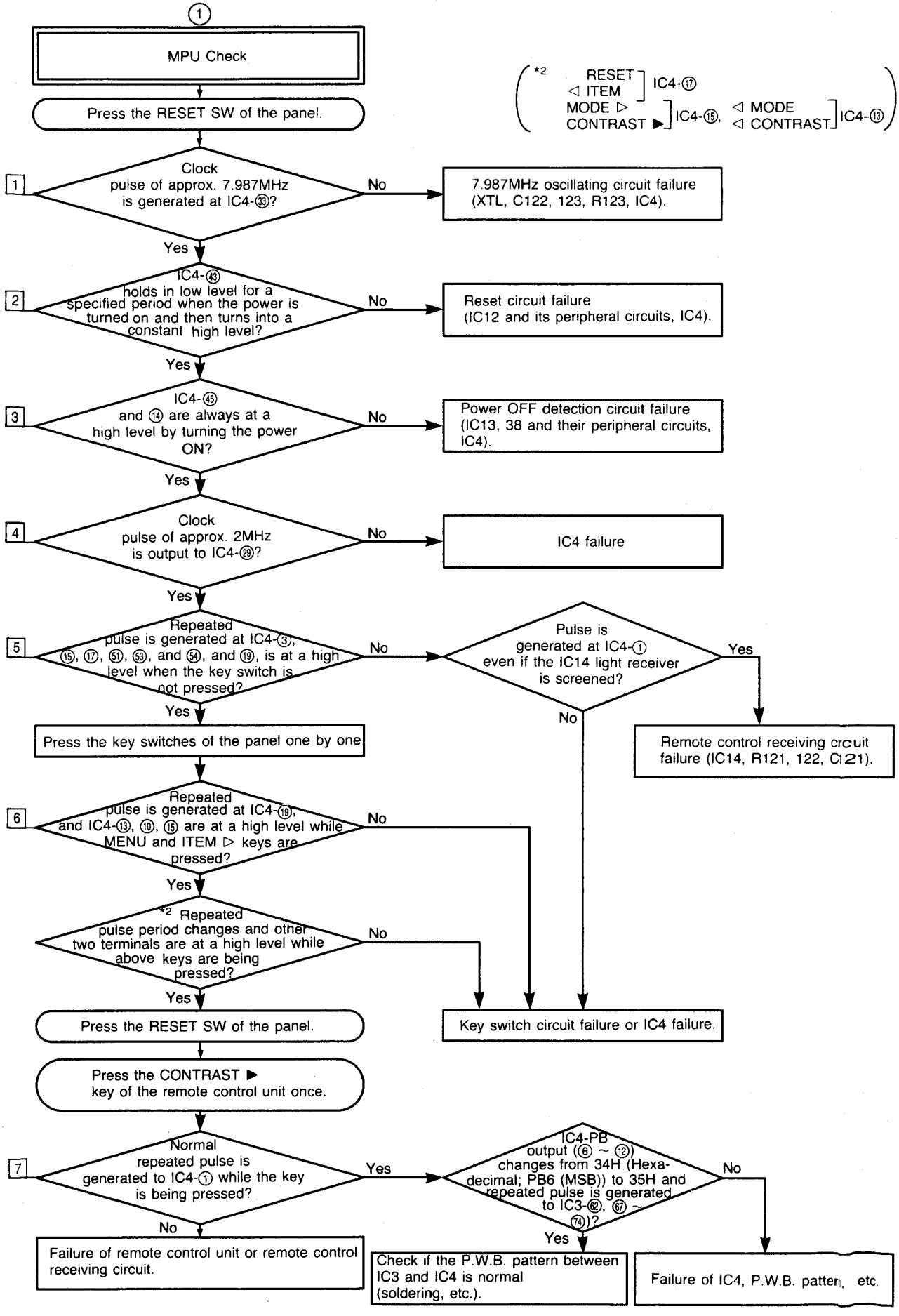
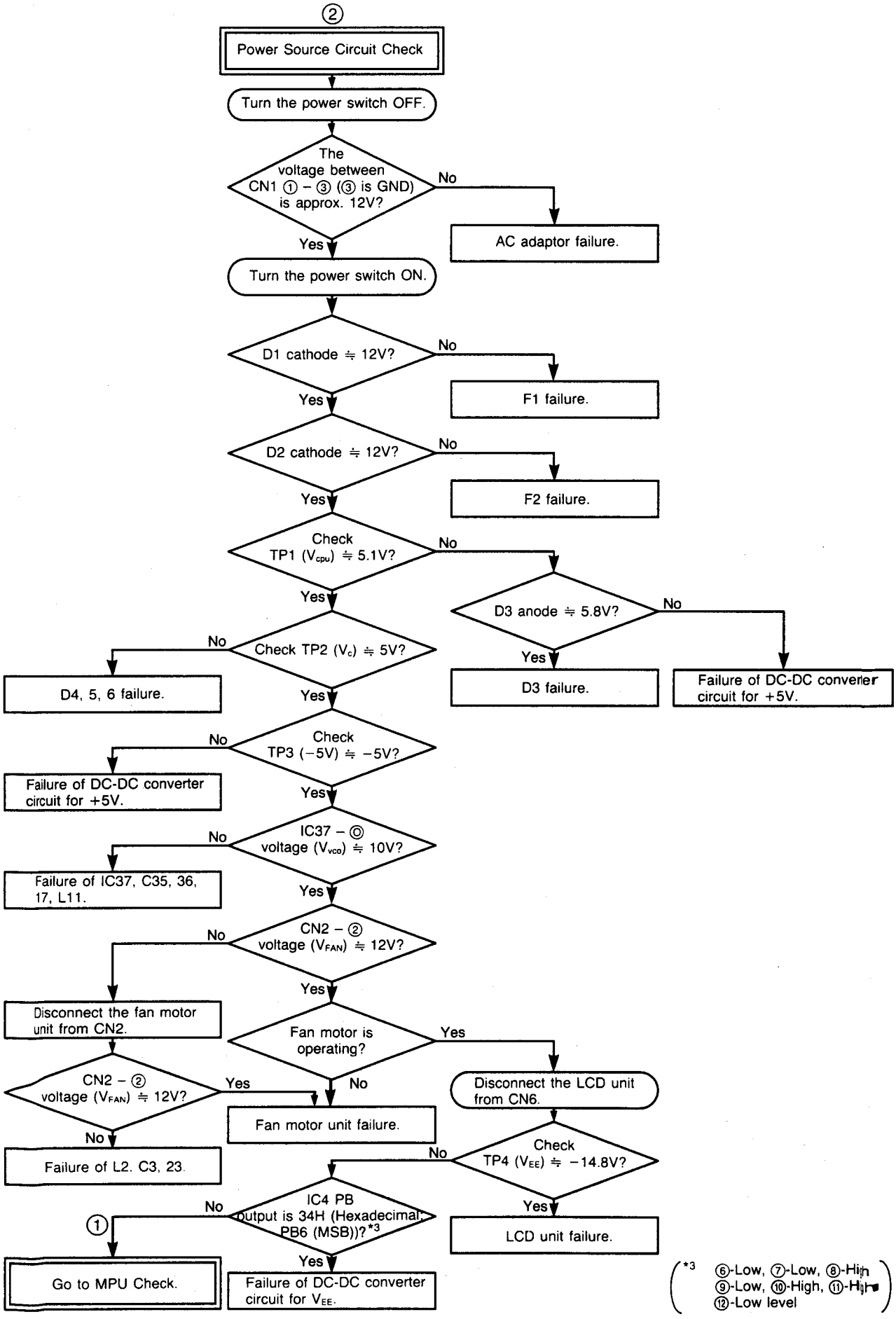


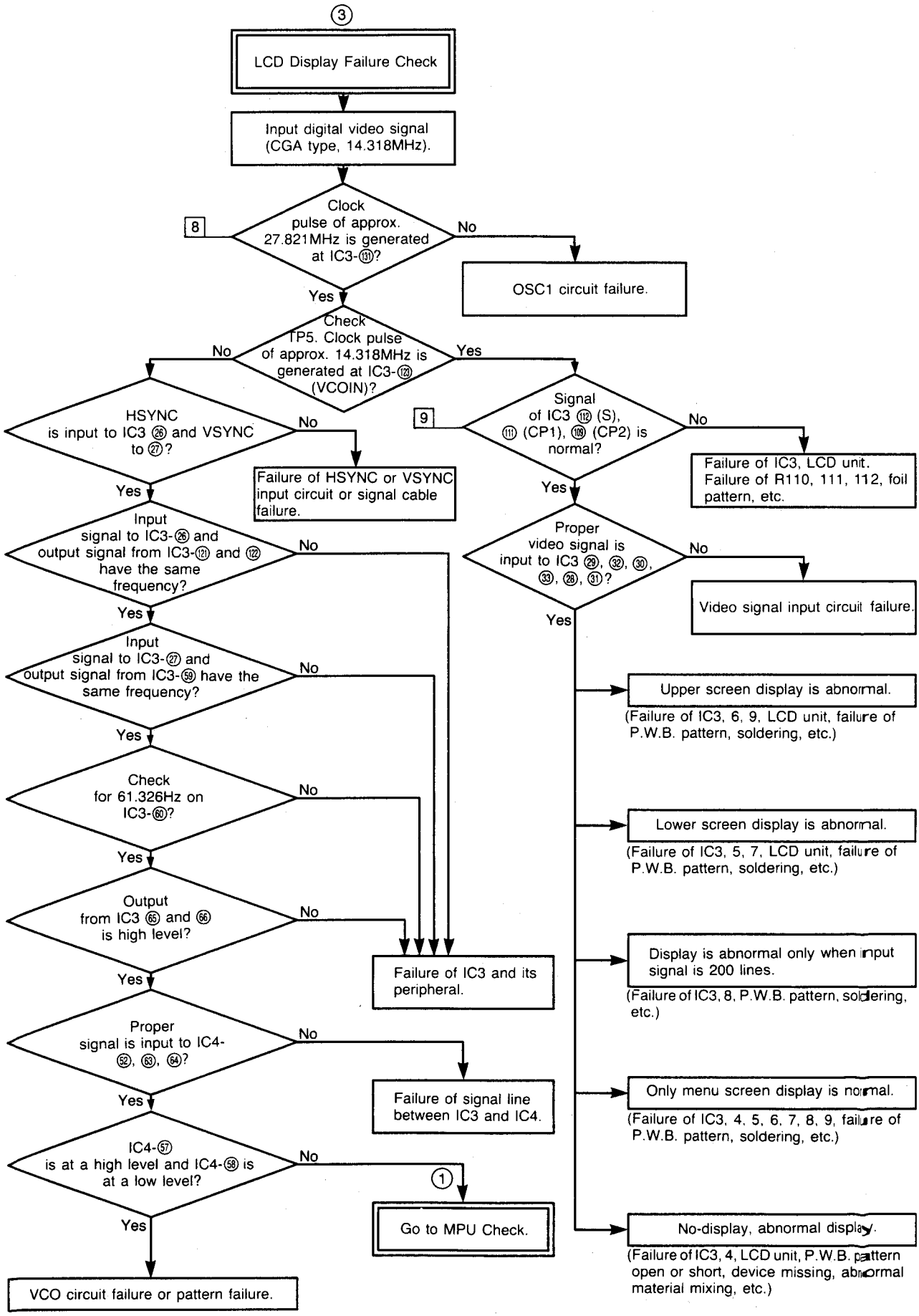
Fig. 26

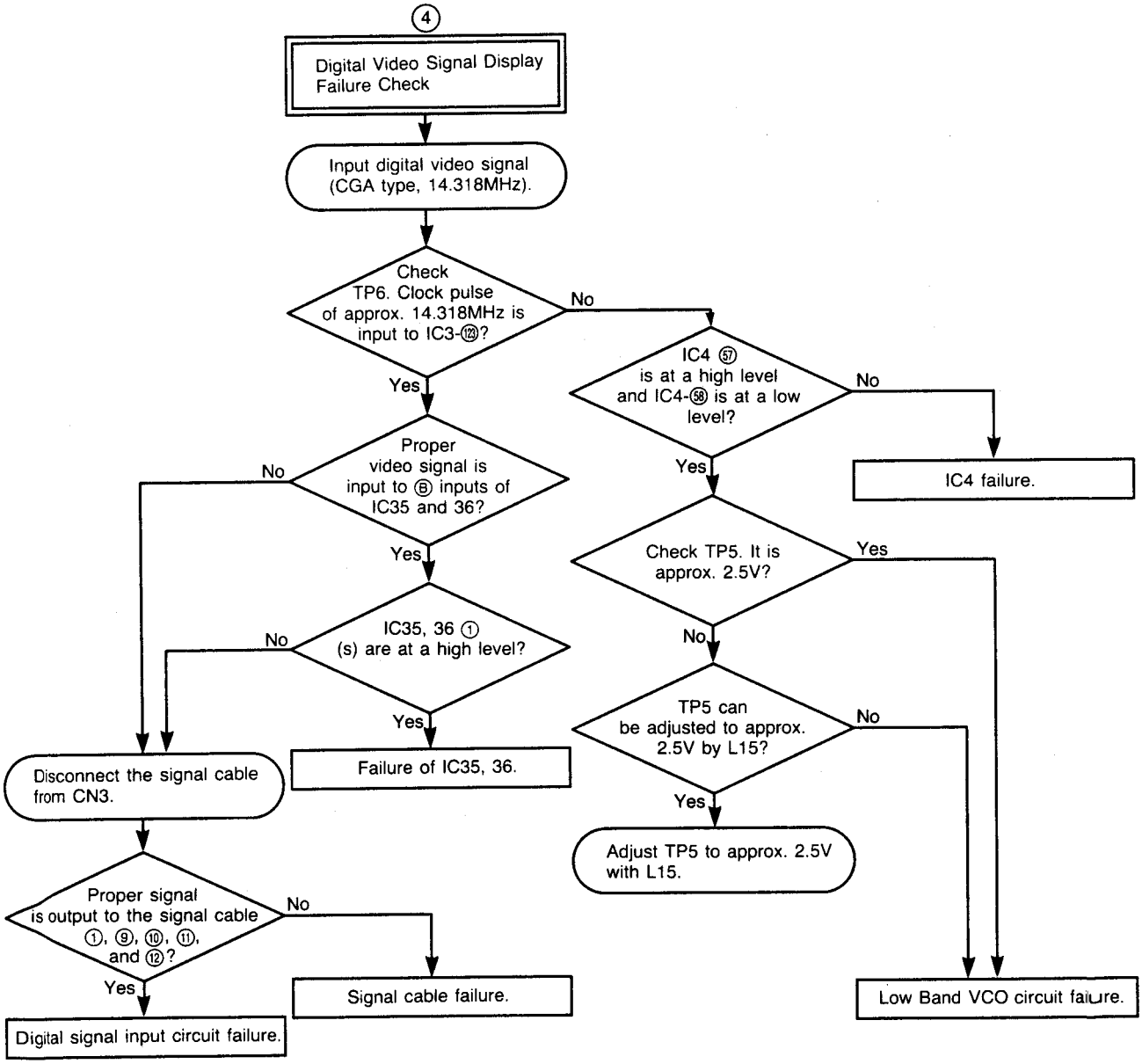
TROUBLESHOOTING CHART

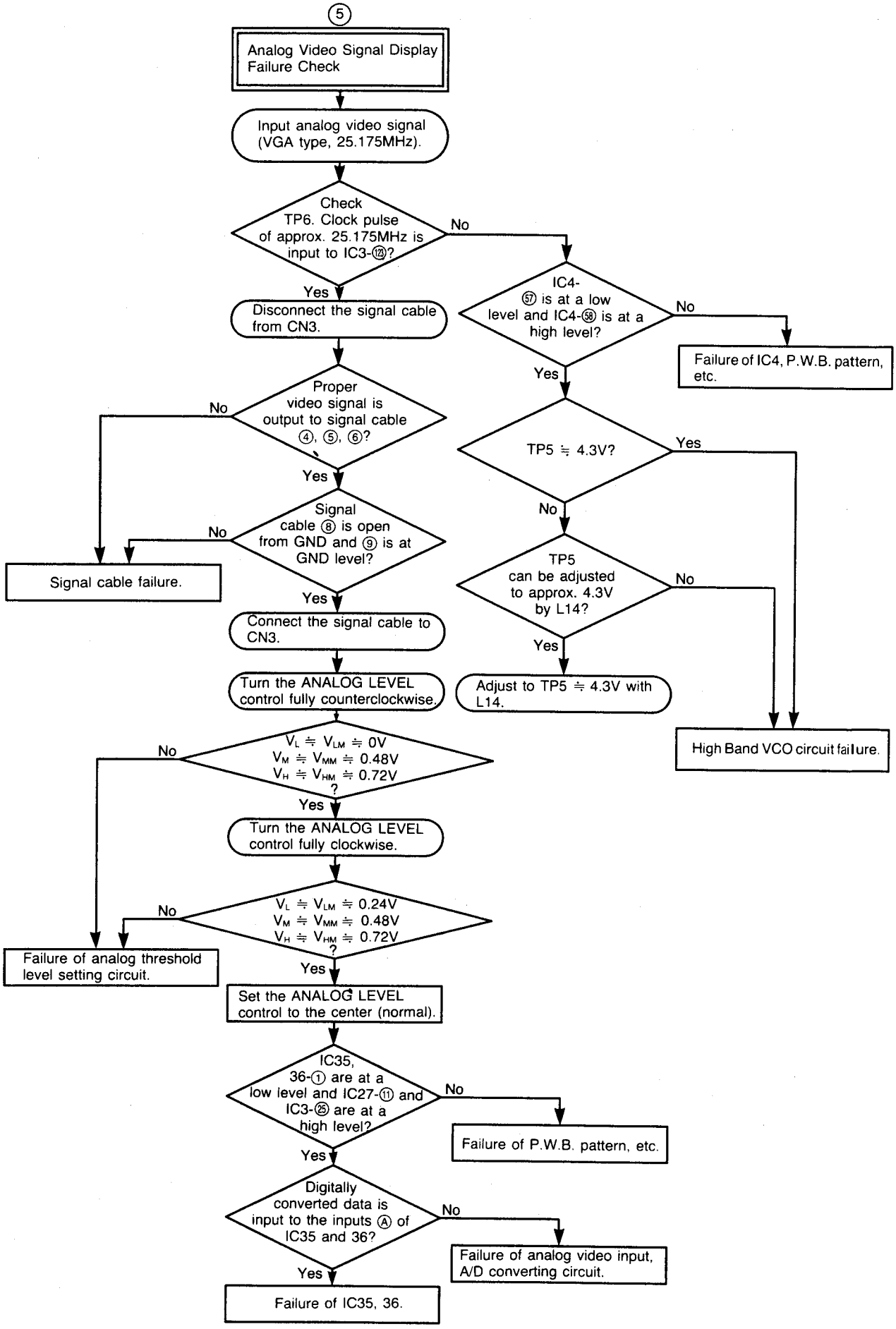


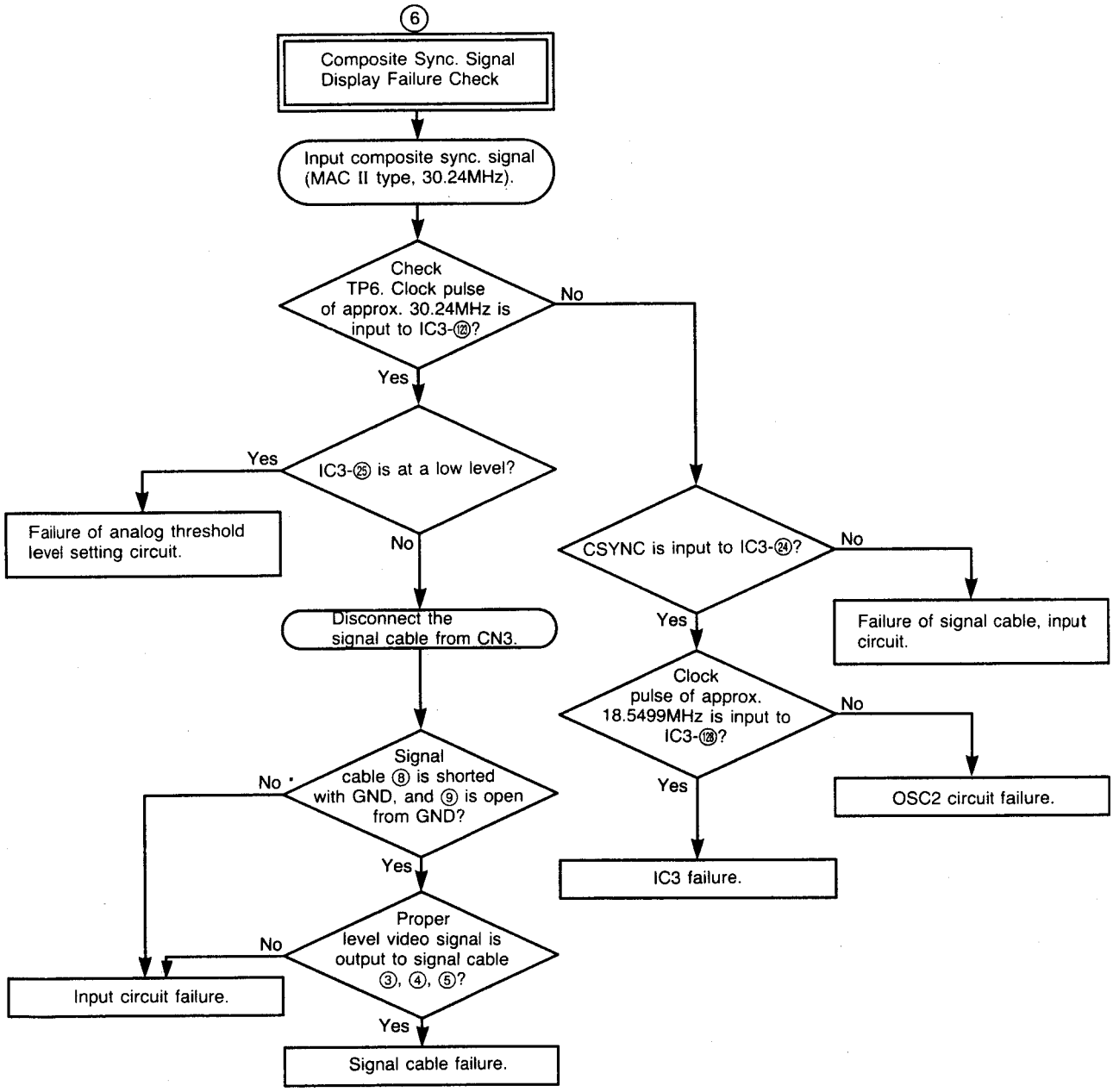

1
MPU Check
Press the RESET SW of the panel.
*2 RESET, ◁ ITEM, MODE ▷, CONTRAST ▶] IC4-⑰
] IC4-⑮, ◁ MODE, ◁ CONTRAST] IC4-⑬
1 Clock pulse of approx. 7.987MHz is generated at IC4-㉝?
No
7.987MHz oscillating circuit failure (XTL, C122, 123, R123, IC4).
Yes
2 IC4-㊸ holds in low level for a specified period when the power is turned on and then turns into a constant high level?
No
Reset circuit failure (IC12 and its peripheral circuits, IC4).
Yes
3 IC4-㊺ and ⑭ are always at a high level by turning the power ON?
No
Power OFF detection circuit failure (IC13, 38 and their peripheral circuits, IC4).
Yes
4 Clock pulse of approx. 2MHz is output to IC4-㉙?
No
IC4 failure
Yes
5 Repeated pulse is generated at IC4-③, ⑮, ⑰, ㊶, ㊸, and ㊹, and ⑲, is at a high level when the key switch is not pressed?
No
Pulse is generated at IC4-① even if the IC14 light receiver is screened?
Yes
Remote control receiving circuit failure (IC14, R121, 122, C121).
No
Yes
Press the key switches of the panel one by one
6 Repeated pulse is generated at IC4-⑲, and IC4-⑬, ⑩, ⑮ are at a high level while MENU and ITEM ▷ keys are pressed?
No
Yes
*2 Repeated pulse period changes and other two terminals are at a high level while above keys are being pressed?
No
Yes
Press the RESET SW of the panel.
Key switch circuit failure or IC4 failure.
Press the CONTRAST ▶ key of the remote control unit once.
7 Normal repeated pulse is generated to IC4-① while the key is being pressed?
Yes
IC4-PB output (⑥ ~ ⑫) changes from 34H (Hexa-decimal; PB6 (MSB)) to 35H and repeated pulse is generated to IC3-㊷, ㊼ ~ ㊹)?
No
No
Failure of remote control unit or remote control receiving circuit.
Yes
Check if the P.W.B. pattern between IC3 and IC4 is normal (soldering, etc.).
Failure of IC4, P.W.B. pattern, etc.

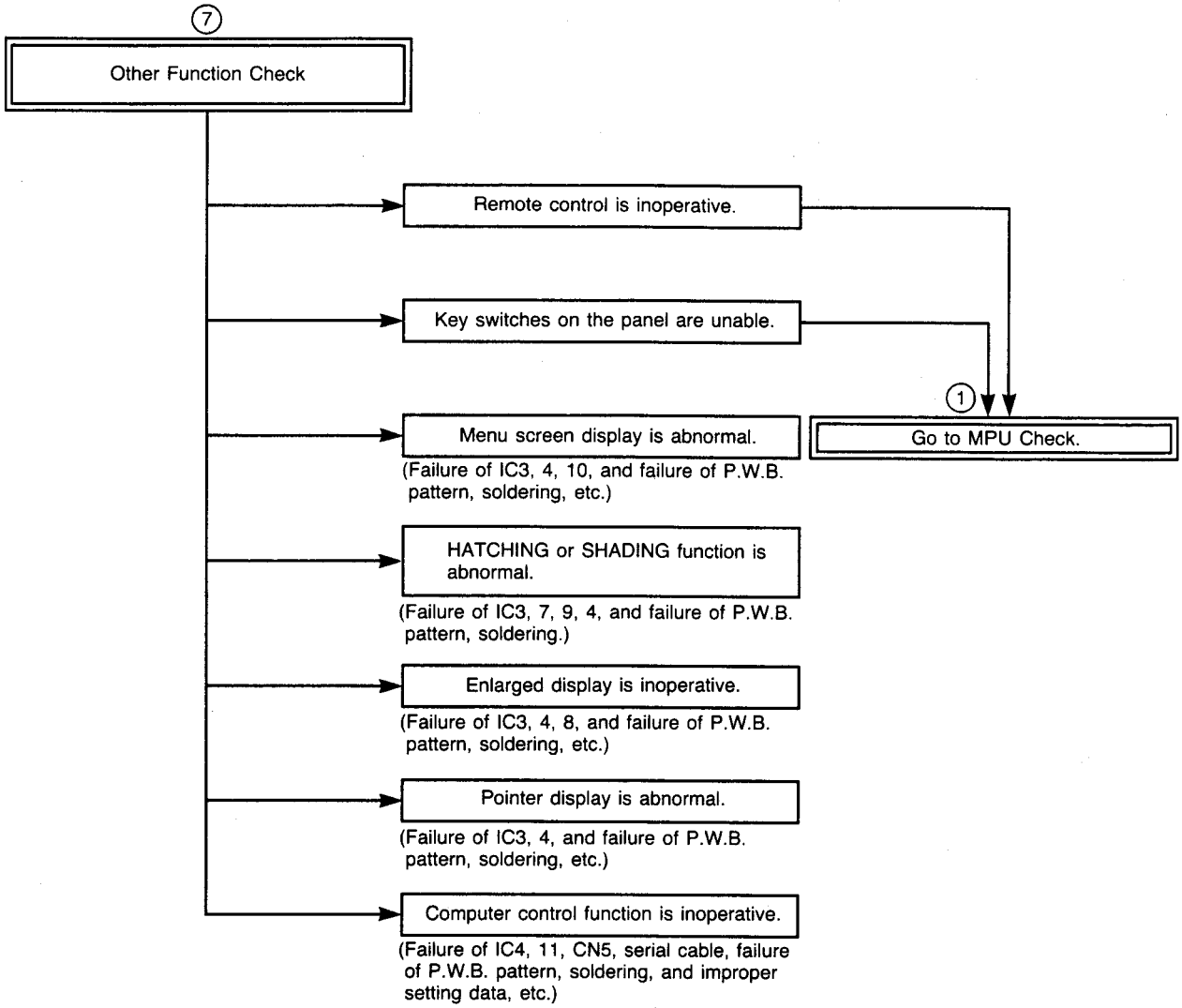

②
Power Source Circuit Check
Turn the power switch OFF.
The voltage between CN1 ① – ③ (③ is GND) is approx. 12V?
No
AC adaptor failure.
Yes
Turn the power switch ON.
D1 cathode ≒ 12V?
No
F1 failure.
Yes
D2 cathode ≒ 12V?
No
F2 failure.
Yes
Check TP1 (V_{cpu}) ≒ 5.1V?
No
D3 anode ≒ 5.8V?
No
Failure of DC-DC converter circuit for +5V.
Yes
D3 failure.
Yes
Check TP2 (V_c) ≒ 5V?
No
D4, 5, 6 failure.
Yes
Check TP3 (−5V) ≒ −5V?
No
Failure of DC-DC converter circuit for +5V.
Yes
IC37 – ⓞ voltage (V_{vco}) ≒ 10V?
No
Failure of IC37, C35, 36, 17, L11.
Yes
CN2 – ② voltage (V_{FAN}) ≒ 12V?
No
Disconnect the fan motor unit from CN2.
CN2 – ② voltage (V_{FAN}) ≒ 12V?
Yes
No
Failure of L2. C3, 23.
Yes
Fan motor is operating?
Yes
No
Fan motor unit failure.
Disconnect the LCD unit from CN6.
Check TP4 (V_{EE}) ≒ −14.8V?
No
Yes
LCD unit failure.
IC4 PB output is 34H (Hexadecimal: PB6 (MSB))?*3
No
①
Go to MPU Check.
Yes
Failure of DC-DC converter circuit for V_{EE}.
(*3 ⑥-Low, ⑦-Low, ⑧-High ⑨-Low, ⑩-High, ⑪-High ⑫-Low level)


③
LCD Display Failure Check
Input digital video signal (CGA type, 14.318MHz).
8
Clock pulse of approx. 27.821MHz is generated at IC3-⑬1?
No
OSC1 circuit failure.
Yes
Check TP5. Clock pulse of approx. 14.318MHz is generated at IC3-⑫8 (VCOIN)?
No
Yes
HSYNC is input to IC3 ㉖ and VSYNC to ㉗?
No
Failure of HSYNC or VSYNC input circuit or signal cable failure.
Yes
Input signal to IC3-㉖ and output signal from IC3-⑫1 and ⑫2 have the same frequency?
No
Yes
Input signal to IC3-㉗ and output signal from IC3-⑤9 have the same frequency?
No
Yes
Check for 61.326Hz on IC3-⑥0?
No
Yes
Output from IC3 ⑥5 and ⑥6 is high level?
No
Yes
Failure of IC3 and its peripheral.
Proper signal is input to IC4-⑤2, ⑤3, ⑥4?
No
Yes
Failure of signal line between IC3 and IC4.
IC4-⑤7 is at a high level and IC4-⑤8 is at a low level?
No
①
Go to MPU Check.
Yes
VCO circuit failure or pattern failure.
9
Signal of IC3 ⑪2 (S), ⑪1 (CP1), ⑩9 (CP2) is normal?
No
Failure of IC3, LCD unit. Failure of R110, 111, 112, foil pattern, etc.
Yes
Proper video signal is input to IC3 ㉙, ㉜, ㉚, ㉝, ㉘, ㉛?
No
Video signal input circuit failure.
Yes
Upper screen display is abnormal.
(Failure of IC3, 6, 9, LCD unit, failure of P.W.B. pattern, soldering, etc.)
Lower screen display is abnormal.
(Failure of IC3, 5, 7, LCD unit, failure of P.W.B. pattern, soldering, etc.)
Display is abnormal only when input signal is 200 lines.
(Failure of IC3, 8, P.W.B. pattern, soldering, etc.)
Only menu screen display is normal.
(Failure of IC3, 4, 5, 6, 7, 8, 9, failure of P.W.B. pattern, soldering, etc.)
No-display, abnormal display.
(Failure of IC3, 4, LCD unit, P.W.B. pattern open or short, device missing, abnormal material mixing, etc.)


④
Digital Video Signal Display Failure Check
Input digital video signal (CGA type, 14.318MHz).
Check TP6. Clock pulse of approx. 14.318MHz is input to IC3-⑫⑧?
No
Yes
IC4 ⑤⑦ is at a high level and IC4-⑤⑧ is at a low level?
No
IC4 failure.
Yes
Proper video signal is input to Ⓑ inputs of IC35 and 36?
No
Yes
Check TP5. It is approx. 2.5V?
Yes
No
IC35, 36 ① (s) are at a high level?
No
Yes
TP5 can be adjusted to approx. 2.5V by L15?
No
Yes
Failure of IC35, 36.
Disconnect the signal cable from CN3.
Adjust TP5 to approx. 2.5V with L15.
Proper signal is output to the signal cable ①, ⑨, ⑩, ⑪, and ⑫?
No
Yes
Signal cable failure.
Low Band VCO circuit failure.
Digital signal input circuit failure.


⑤
Analog Video Signal Display Failure Check
Input analog video signal (VGA type, 25.175MHz).
Check TP6. Clock pulse of approx. 25.175MHz is input to IC3-⑫?
No
Yes
Disconnect the signal cable from CN3.
IC4-⑰ is at a low level and IC4-⑱ is at a high level?
No
Failure of IC4, P.W.B. pattern, etc.
Yes
Proper video signal is output to signal cable ④, ⑤, ⑥?
No
Yes
TP5 ≒ 4.3V?
Yes
No
Signal cable ⑧ is open from GND and ⑨ is at GND level?
No
Yes
TP5 can be adjusted to approx. 4.3V by L14?
No
Yes
Signal cable failure.
Connect the signal cable to CN3.
Adjust to TP5 ≒ 4.3V with L14.
High Band VCO circuit failure.
Turn the ANALOG LEVEL control fully counterclockwise.
$V_L \fallingdotseq V_{LM} \fallingdotseq 0V$
$V_M \fallingdotseq V_{MM} \fallingdotseq 0.48V$
$V_H \fallingdotseq V_{HM} \fallingdotseq 0.72V$
?
No
Yes
Turn the ANALOG LEVEL control fully clockwise.
$V_L \fallingdotseq V_{LM} \fallingdotseq 0.24V$
$V_M \fallingdotseq V_{MM} \fallingdotseq 0.48V$
$V_H \fallingdotseq V_{HM} \fallingdotseq 0.72V$
?
No
Yes
Failure of analog threshold level setting circuit.
Set the ANALOG LEVEL control to the center (normal).
IC35, 36-① are at a low level and IC27-⑪ and IC3-㉕ are at a high level?
No
Yes
Failure of P.W.B. pattern, etc.
Digitally converted data is input to the inputs Ⓐ of IC35 and 36?
No
Yes
Failure of analog video input, A/D converting circuit.
Failure of IC35, 36.


⑥
Composite Sync. Signal Display Failure Check
Input composite sync. signal (MAC II type, 30.24MHz).
Check TP6. Clock pulse of approx. 30.24MHz is input to IC3-⑫⑧?
No
Yes
IC3-㉕ is at a low level?
Yes
Failure of analog threshold level setting circuit.
No
Disconnect the signal cable from CN3.
Signal cable ⑧ is shorted with GND, and ⑨ is open from GND?
No
Yes
Proper level video signal is output to signal cable ③, ④, ⑤?
No
Input circuit failure.
Yes
Signal cable failure.
CSYNC is input to IC3-㉔?
No
Failure of signal cable, input circuit.
Yes
Clock pulse of approx. 18.5499MHz is input to IC3-⑫⑧?
No
OSC2 circuit failure.
Yes
IC3 failure.


⑦
Other Function Check
Remote control is inoperative.
Key switches on the panel are unable.
①
Go to MPU Check.
Menu screen display is abnormal.
(Failure of IC3, 4, 10, and failure of P.W.B. pattern, soldering, etc.)
HATCHING or SHADING function is abnormal.
(Failure of IC3, 7, 9, 4, and failure of P.W.B. pattern, soldering.)
Enlarged display is inoperative.
(Failure of IC3, 4, 8, and failure of P.W.B. pattern, soldering, etc.)
Pointer display is abnormal.
(Failure of IC3, 4, and failure of P.W.B. pattern, soldering, etc.)
Computer control function is inoperative.
(Failure of IC4, 11, CN5, serial cable, failure of P.W.B. pattern, soldering, and improper setting data, etc.)

[1] IC4-㉝ ... 1V/div

50ns/div

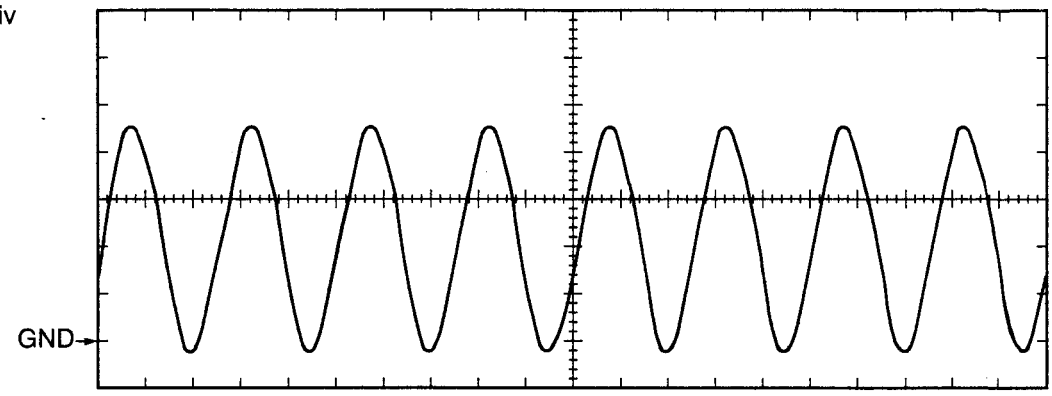


Fig. 27

[2] V_{cpu} ... 2V/div
IC4-㊸ ... 2V/div

50ms/div

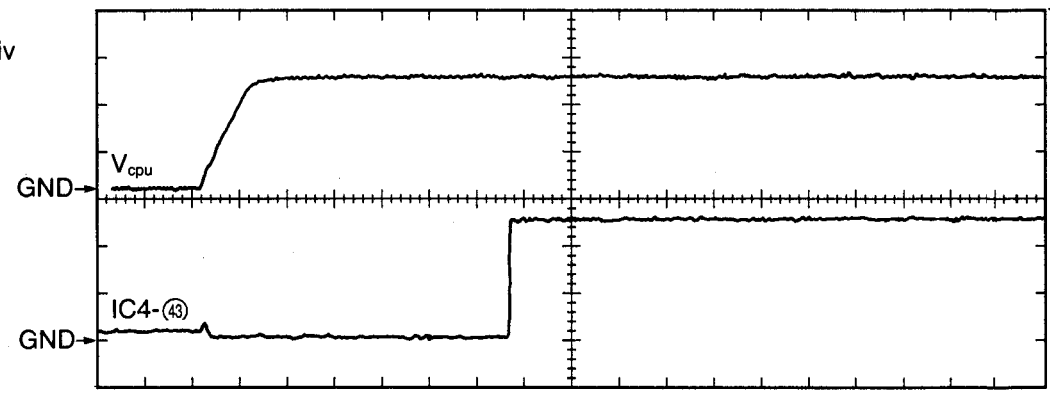


Fig. 28

[3] V_{cpu} ... 2V/div
IC4-㊺ or ⑭ ... 2V/div

10ms/div

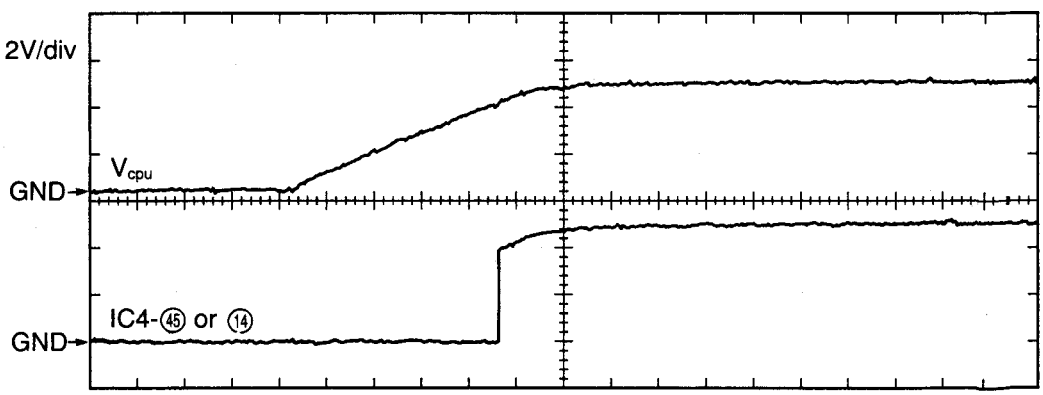


Fig. 29

[4] IC4-㉙ ... 1V/div

100ns/div

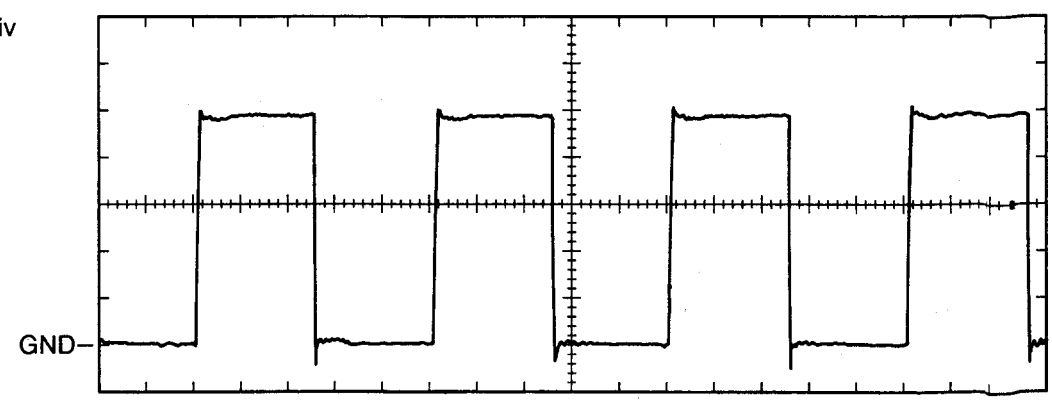


Fig. 30

5 IC4-⑬⑮⑰㉛㉝㉟
... 1V/div

200μs/div

(SW OFF)

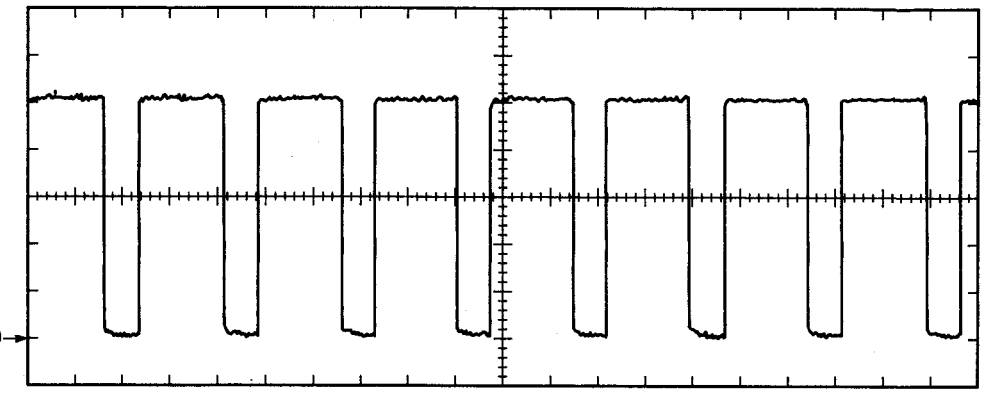


Fig. 31

6 IC4-⑬⑮⑰⑲
... 1V/div

200μs/div

(SW ON)

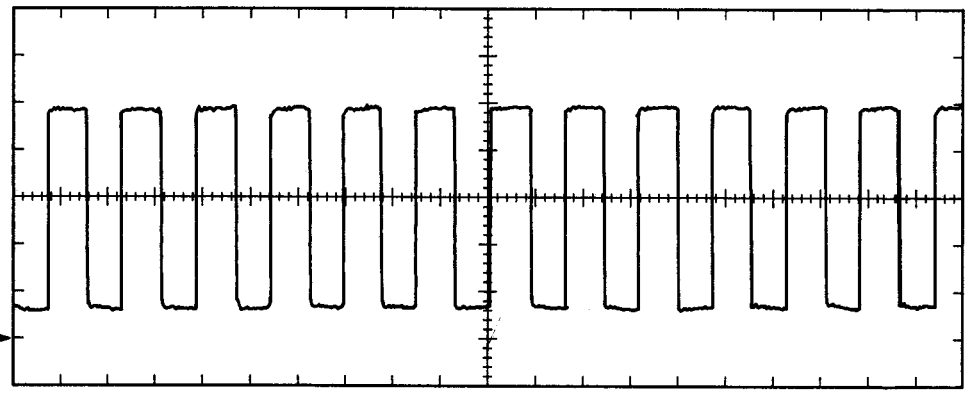


Fig. 32

7 IC4-① ... 1V/div

2ms/div

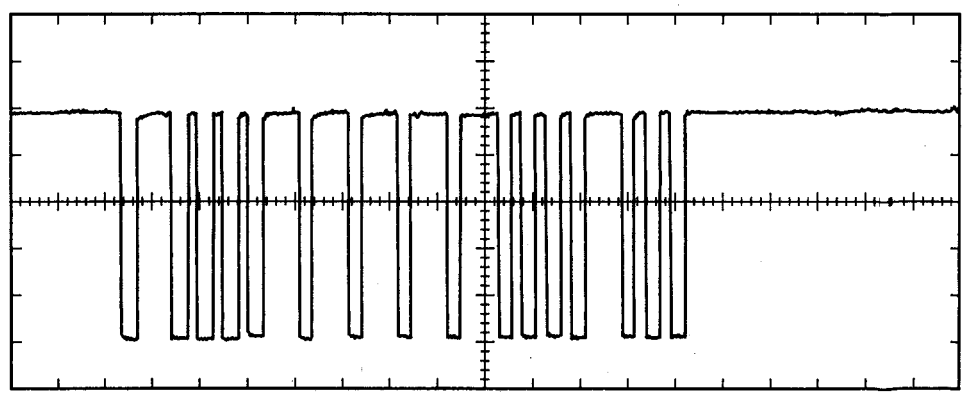


Fig. 33

8 IC3-⑬① ... 1V/div

10ns/div

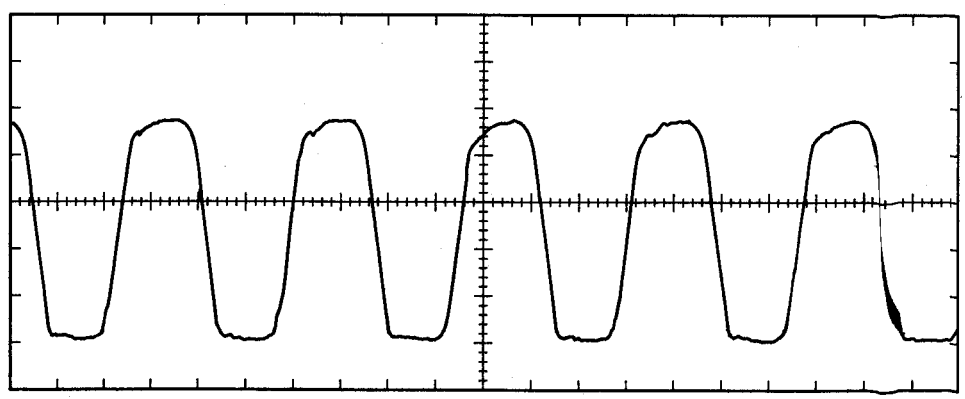


Fig. 34

9 IC3-⑪ (CP1)
... 1V/div

10μs/div

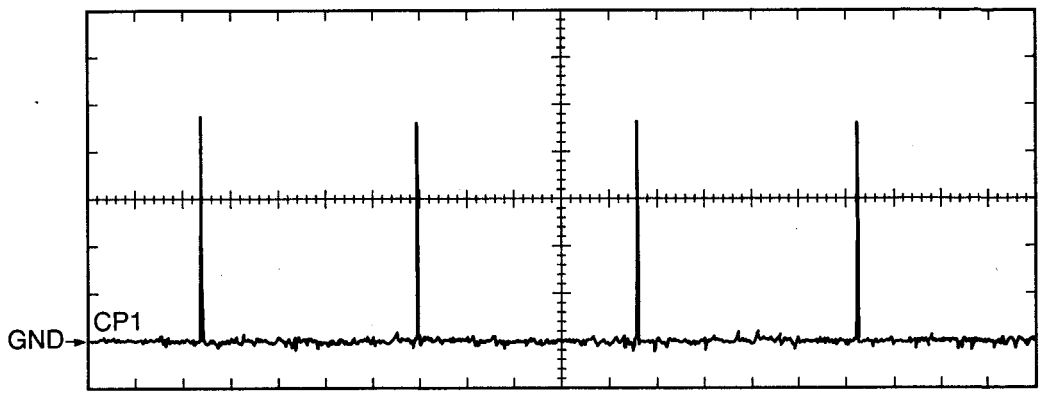


Fig. 35

IC3-⑪ (CP1)
... 2V/div
IC3-⑩ (CP2)
... 2V/div

100ns/div

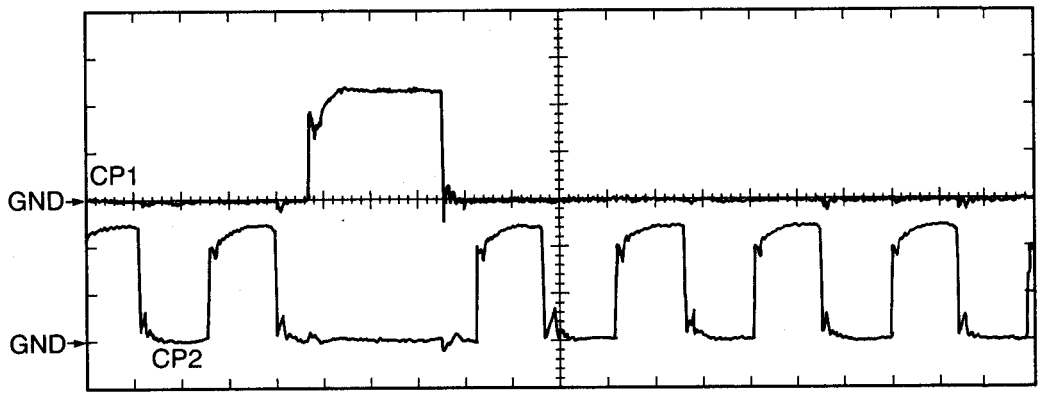


Fig. 36

IC3-⑫ (S)
... 2V/div
IC3-⑩ (CP2)
... 2V/div

100ns/div

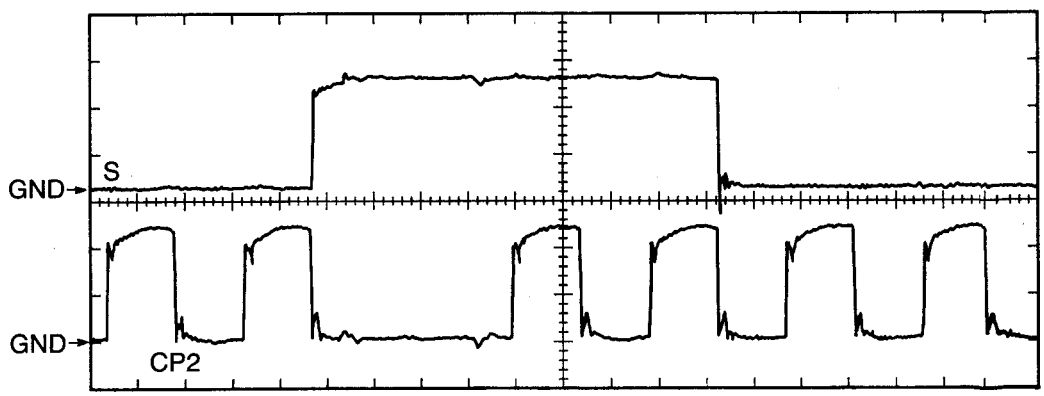
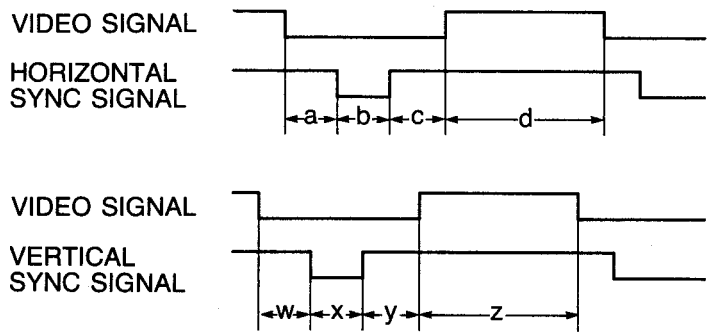
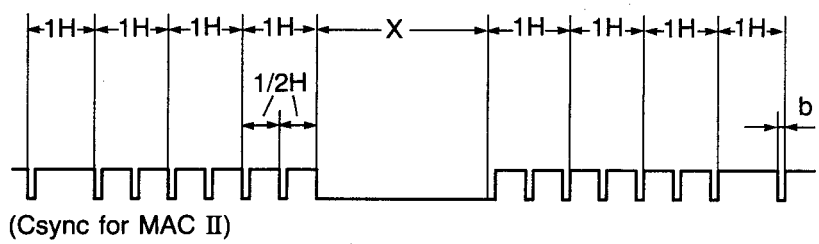


Fig. 37

TIMING CHART

■ The following timing charts are applied to Tables 15, 16 and 17.





(Csync for MAC II)

Fig. 38

Table 15

			1	2	3	4	5	6	7	8
			IBM				IBM		IBM	IBM
			VGA	VGA/MCGA		VGA	EGA		CGA	MDA
							Text 40chr	80chr/Graphic	40chr, Graphic/80chr	
			720 dot	640 dot			640 dot		640 dot	720 dot
			400 line	400 line	350 line	480 line	350 line		200 line	350 line
Hsync	FRONT PORCH a	dot	18	16			−7	−3	95/103	9
	SYNC b	dot	108	96			80	80	64/ 48	144
	BACK PORCH c	dot	54	48			39	27	113/121	9
	VIDEO PERIOD d	dot	720	640			640	640	640	720
	1H (a+b+c+d)	dot	900	800			752	744	912	882
		μs	31.777417	31.777557			46.256997	45.764901	63.696047	54.253552
	1 dot	ns	35.308241	39.721946			61.511964	61.511964	69.842157	61.511964
	1/H	KHz	31.468906	31.468881			21.618351	21.850806	15.699561	18.432197
	1/dot	MHz	28.322	25.175			16.257		14.318	16.257
	LEVEL		TTL	TTL			TTL		TTL	TTL
	SYNC POLARITY	+/−	−	−	+	−	+		+	+
Vsync	FRONT PORCH W	H	13	13	38	11	1		25	0
	SYNC X	H	2	2	2	2	13		3	16
	BACK PORCH Y	H	34	34	59	32	2		34	4
	VIDEO PERIOD Z	H	400	400	350	480	350		200	350
	1V (W+X+Y+Z)	H	449	449	449	525	366	366	262	370
		ms	14.26806	14.268123	14.268123	16.683217	16.930061	16.749954	16.688364	20.073814
	1/V	Hz	70.00	70.00	70.00	59.94	59.07	59.70	59.92	49.82
	LEVEL		TTL	TTL	TTL	TTL	TTL		TTL	TTL
	SYNC	+/−	+	+	−	−	−		+	−
VIDEO	LEVEL		0.7Vp-p MAX 75Ω Load				TTL		TTL	TTL
	TYPE		R, G, B				R, G, B r, g, b		R, G, B I	Mono Video I
REMARKS									• AUTO SETUP shall be set in the 40chr-graphic mode.	

Table 16

			9	10	11	12	13	14	15	
			Hercules		Hercules		APPLE		AT & T	
			HGC/HGC+		Incolor		MAC II Video Card	MAC +/SE	6300WGS	
			Text	Graphic	Text	Graphic				
			720 dot		720 dot		640 dot	512 dot	640 dot	
			350 line	348 line	350 line	348 line	480 line	342 line	350 line	400 line
Hsync	FRONT PORCH a	dot	7	−2	7	−2	64	15	78	
	SYNC b	dot	135	112	135	112	64	64	104	
	BACK PORCH c	dot	20	34	20	34	96	113	106	
	VIDEO PERIOD d	dot	720	720	720	720	640	512	640	
	1H (a+b+c+d)	dot	882	864	882	864	864	704	928	
		μs	55.125	54.000	46.42105	45.473684	28.571429	44.934641	38.666667	
	1 dot	ns	62.500		52.631579		33.068783	63.827614	41.666667	
	1/H	KHz	18.1406	18.5185	21.54195	21.990741	35.000	22.254545	25.862069	
	1/dot	MHz	16.000		19.000		30.240	15.6672	24.000	
	LEVEL		TTL		TTL		TTL	TTL	TTL	
	SYNC POLARITY	+/−	+		+		−	+	+	
Vsync	FRONT PORCH W	H	0		0		3	0	25	0
	SYNC X	H	16		16		3	4	16	16
	BACK PORCH Y	H	4	6	4	6	39	24	41	16
	VIDEO PERIOD Z	H	350	348	350	348	480	342	350	400
	1V (W+X+Y+Z)	H	370	370	370	370	525	370	432	
		ms	20.39625	19.980	17.175789	16.825263	15.000	16.625817	16.704	
	1/V	Hz	49.03	50.05	58.22	59.43	66.68	60.15	59.87	
	LEVEL		TTL		TTL		TTL	TTL	TTL	
	SYNC	+/−	−		−		−	+	+	
VIDEO	LEVEL		TTL		TTL		1.0Vp-p MAX 75Ω Load	TTL	TTL	
	TYPE		Mono Video I		R, G, B r, g, b		R, G, B	R, G, B I	R, G, B I	
REMARKS							● Signal cable is required. ● Synchronous signal is Csync.	● A/D converter adaptor is required.	● Signal cable is required. ● Operates in the 400 line mode also with 350 line signal input.	

Table 17

			16	17	18	19	20	21	22	23
			APPLE	NEC		SHARP				
			APPLE IIe/ +/c/GS	PC-9801		AX-286 AX-386				
			560 dot	640 dot		640 dot				
			192 line	200 line	400 line	480 line				
Hsync	FRONT PORCH a	dot	109	59	59	18				
	SYNC b	dot	170	64	64	88				
	BACK PORCH c	dot	73	133	85	86				
	VIDEO PERIOD d	dot	560	640	640	640				
	1H (a+b+c+d)	dot	912	896	848	832				
		μs	63.696047	62.578572	40.280060	33.048659				
	1 dot	ns	69.842157	69.842157	47.500071	39.721946				
	1/H	KHz	15.699561	15.979911	24.826179	30.258				
	1/dot	MHz	14.318	14.318	21.0526	25.175				
	LEVEL		TTL	TTL		TTL				
	SYNC POLARITY	+/−	+	−		+				
Vsync	FRONT PORCH W	H	33	15	7	4				
	SYNC X	H	3	8	8	12				
	BACK PORCH Y	H	34	37	25	5				
	VIDEO PERIOD Z	H	192	200	400	480				
	1V (W+X+Y+Z)	H	262	260	440	501				
		ms	16.688364	16.270429	17.723227	16.557379				
	1/V	Hz	59.92	61.46	56.42	60.40				
	LEVEL		TTL	TTL		TTL				
	SYNC	+/−	+	−		−				
VIDEO	LEVEL		TTL	TTL		TTL				
	TYPE		R, G, B I	R, G, B I		R, G, B r, g, b				
REMARKS			Composite signal-responsive A/D converter adaptor is separately required. Shall be operated in the IBM CGA mode.	Signal cable is required.						

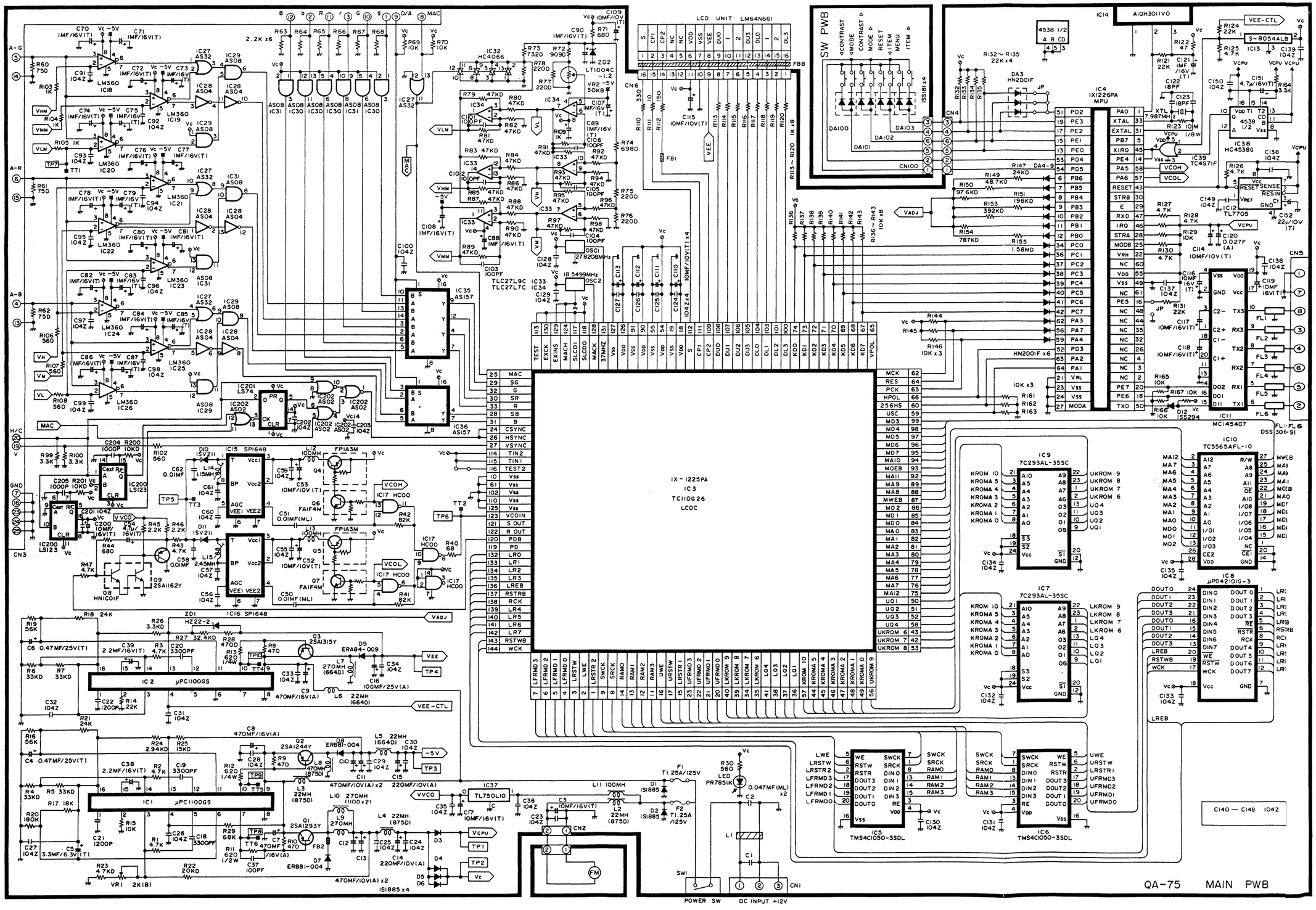


Fig. 39 CIRCUIT DIAGRAM

for SEC: Serial No. 1 ~ 810, 838, 839, 840

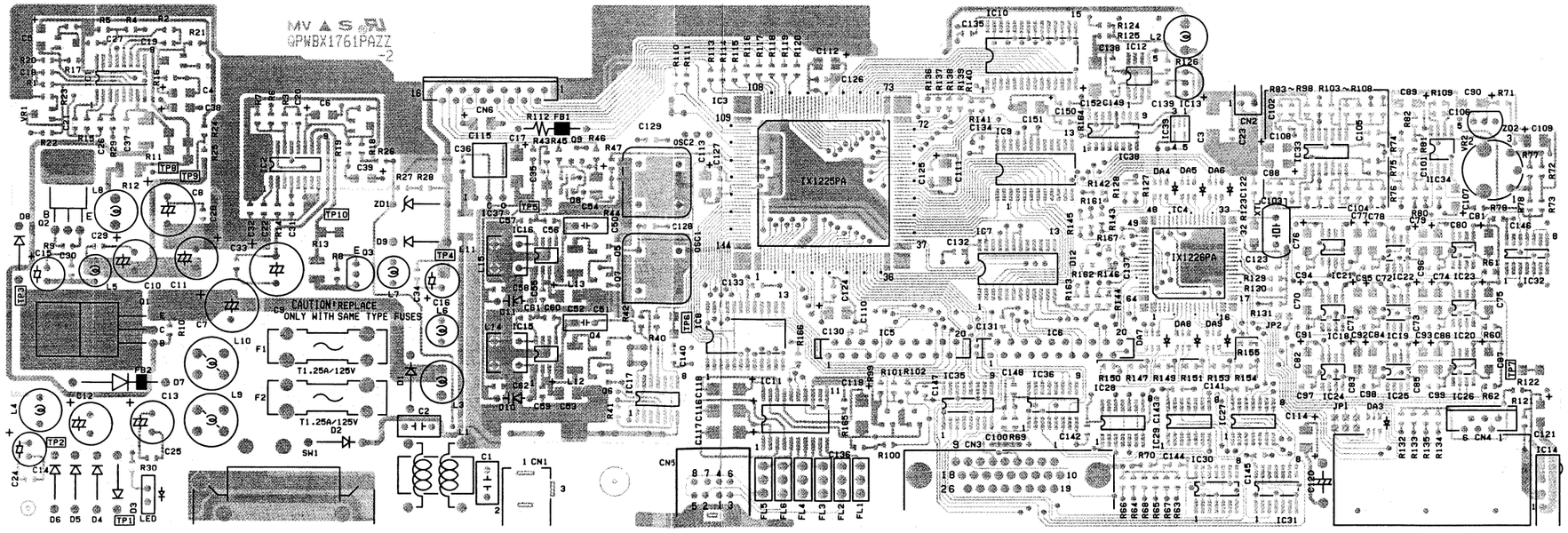


Fig. 40 P.W.B. PATTERN (TYPE A)

for SEC : Serial No. 811 ~ 2300 except for 838, 839, 840
for SECL: Serial No. 1 ~ 350

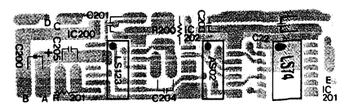


Fig. 41 P.W.B. PATTERN (TYPE B)

for SEC : Serial No. 2301 ~
for SECL : Serial No. 351 ~
for SEEG: Serial No. 1 ~

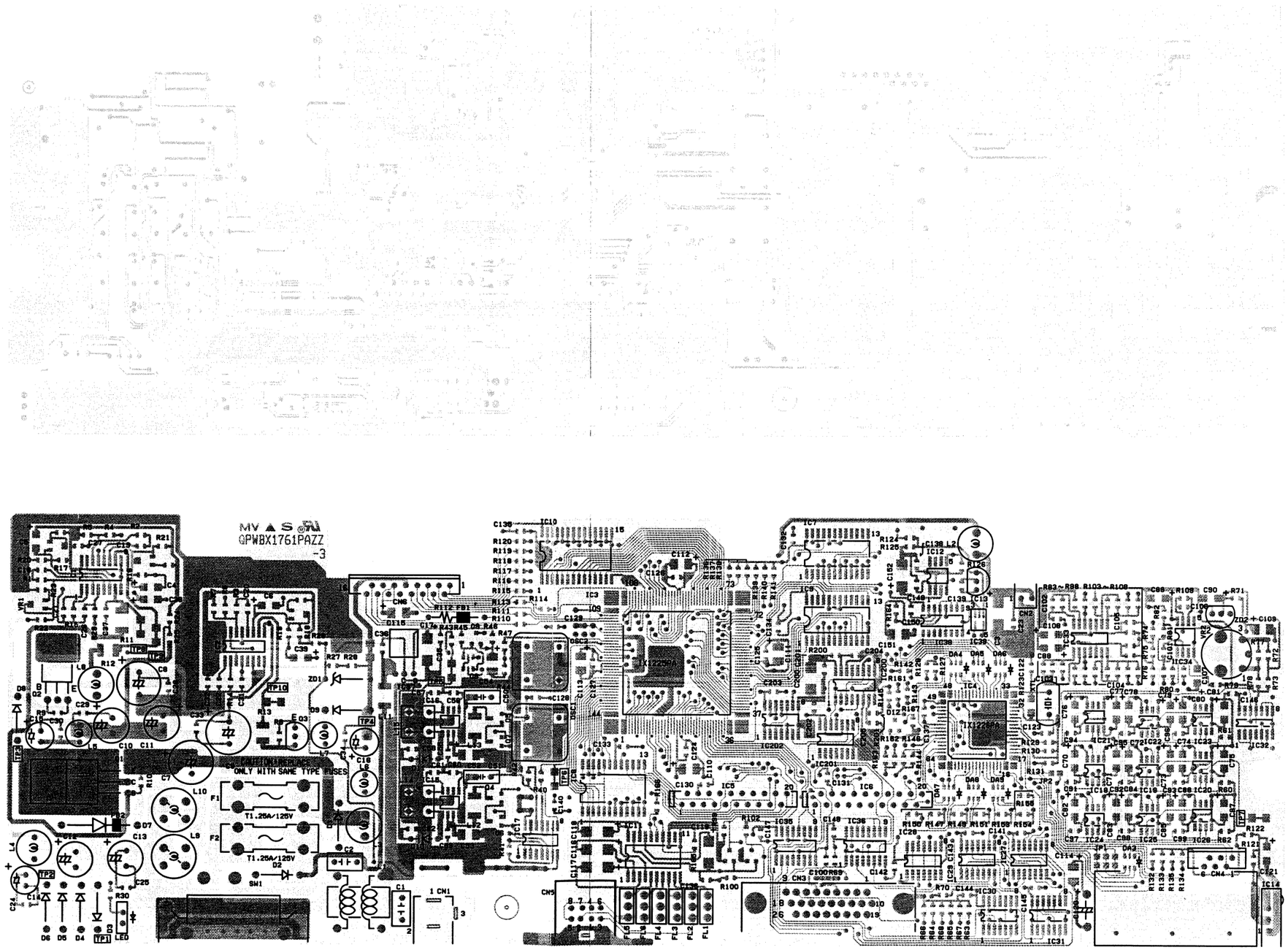


Fig. 42 P.W.B. PATTERN (TYPE C)

FOR SEEG SERVICE ENGINEERS

① This supplement manual contains following informations.

② Please replace P.61 ~ 64 with this supplement manual, because QA-75 for SEEG has Type D MAIN P.W.B. from serial No.1, so only Type D P.W.B. informations are available for SEEG service engineers.

③ Type D circuit also contains the design change described in P.77.

CHANGED REPLACEMENT PARTS FOR TYPE D

Please correct REPLACEMENT PARTS LIST in accordance with following table.

ELECTRIC PARTS

NO.	REF. NO.	PARTS CODE	NEW	DESCRIPTION	QTY	PRICE
1. Resistor						
1-1	R40, 204, 205, 214~219	VRS-TW2AD680J		TW)1/10W-68J	1→9	AA
1-2	R44, 71, 113~120	VRS-TW2AD681J		TW)1/10W-680J	2→10	AA
1-3	R99, 100, 164, 202	VRS-TW2AD332J		TW)1/10W-3.3KJ	3→4	AA
1-4	R103~105, 109	VRS-TW2AD102J		TW)1/10W-1KJ	12→4	AA
1-5	R111, 203	VRS-TW2AD100J		TW)1/10W-10J	1→2	AA
1-6	R206~213	VRS-TW2AD221J		TW)1/10W-220J	0→8	AA
1-7		VRD-ST2DF151J		ST)1/5S-150J	1→0	—
2. Capacitor						
2-1	C2	RC-QZS473AFYK		FILM 0.047μF/K/50V	2→1	AF
2-2	C206~213	VCCCTV1H3470J		CERAMIC CH/47pF/J/50V	0→8	AA
2-3	C237~239	RC-CZ0303PAZZ		CERAMIC 104Z	0→3	AA
3. Coil						
3-1	L1	RTTNZ0389PAZZ	N	FERRITE CORE	0→1	AH
3-2		RTRNZ0306PAZZ		FERRITE CORE	1→0	—
4. Core, Filter						
4-1	FB3	RCORF0061PAZZ	N	FERRITE CHIP	0→1	AB
4-2	FB4	RCORF0062PAZZ	N	BEAD FILTER	0→1	AB
4-3	FL7	RFILN0005PAZZ	N	ZJSC-R47-181	0→1	AD

CABINET PARTS

5-1		DCABA0472AASA	N	CABINET ASSEMBLY A	1→0	—
5-2		DCABA0478AASA	N	CABINET ASSEMBLY A	0→1	BH
5-3		DCABB0019AASA	N	CABINET ASSEMBLY B	1→0	—
5-4		DCABB0020AASA	N	CABINET ASSEMBLY B	0→1	BB

OTHERS

6-1		PSPAK0040PAZZ		LED SPASER	0→4	AA
6-2		TLABZ0466PAZZ	N	PET TAPE	0→1	AC

NOT REPLACEMENT ITEM

7-1		DPWB-1006PAZZ	N	MAIN P.W.B. ASSEMBLY	1→0	—
7-2		DPWB-1030PAZZ	N	MAIN P.W.B. ASSEMBLY	0→1	CZ

REPLACEMENT PARTS LIST

"HOW TO ORDER REPLACEMENT PARTS"

To have your order filled promptly and correctly, please furnish the following information.

1. MODEL NUMBER
2. REF. NO.
3. PART NO.
4. DESCRIPTION

ELECTRIC PARTS

NO.	REF. NO.	PARTS CODE	NEW	DESCRIPTION	QTY	PRICE
1. LCD, FAN						
1-1	LCD	DUNTL0052PAZZ	N	LCD UNIT (LM64N661)	1	CM
1-2	FAN	RMOTV0003PAZZ	N	FAN MOTOR	1	BF
2. IC						
2-1	IC1, 2	RH-IX1234PAZZ	N	μPC1100GS (T)	2	AL
2-2	IC3	RH-IX1225PAZZ	N	TC110G26	1	BF
2-3	IC4	RH-IX1226PAZZ	N	MC68HC11A8FU	1	AY
2-4	IC5, 6	RH-IX1232PAZZ	N	TMS4C1050-3SDL	2	BK
2-5	IC7, 9	RH-IX1229PAZZ	N	CY7C293AL-35SC	2	AY
2-6	IC8	RH-IX1230PAZZ	N	μPD42101G-3	1	AW
2-7	IC10	RH-IX1231PAZZ	N	TC5565AFL-10	1	AT
2-8	IC11	RH-IX1228PAZZ	N	MC145407DW	1	AP
2-9	IC12	RH-IX0855PAZZ		TL7705CPS-B	1	AK
2-10	IC13	RH-IX0847PAZZ		S-8054ALB	1	AE
2-11	IC14	FHIC-K02-KA90		U0002KAZZ (RECEIVER)	1	AH
2-12	IC15, 16	RH-IX1235PAZZ	N	SP1648MPT (T)	2	AT
2-13	IC17	RH-IX1239PAZZ	N	MM74HC00M (T)	1	AE
2-14	IC18~26	RH-IX1238PAZZ	N	LM360M (T)	9	AK
2-15	IC27	RH-IX1243PAZZ	N	SN74AS32NS (T)	1	AE
2-16	IC28	RH-IX1241PAZZ	N	SN74AS04NS (T)	1	AE
2-17	IC29~31	RH-IX1240PAZZ	N	SN74AS08NS (T)	3	AE
2-18	IC32	RH-IX1244PAZZ	N	μPD74HC4066G (T)	1	AE
2-19	IC33	RH-IX1236PAZZ	N	TLC27L9CNS (T)	1	AR
2-20	IC34	RH-IX1237PAZZ	N	TLC27L7CPS (T)	1	AN
2-21	IC35, 36	RH-IX1242PAZZ	N	SN74AS157NS (T)	2	AH
2-22	IC37	RH-IX1233PAZZ	N	TL750L10CLP	1	AM
2-23	IC38	RH-IX1260PAZZ	N	μPD74HC4538G-E1	1	AG
2-24	IC39	VHITC4S71F/-1	N	TC4S71FTE85R	1	AC
2-25	IC200	RH-IX1284PAZZ	N	SN74LS123NS	1	AE
2-26	IC201	RH-IX1133PAZZ		SN74LS74NS	1	AD
2-27	IC202	RH-IX1285PAZZ	N	SN74AS02NS	1	AD

ELECTRIC PARTS

NO.	REF. NO.	PARTS CODE	NEW	DESCRIPTION	QTY	PRICE
3. Transistor						
3-1	Q1	VS2SA1293Y/1E	N	2SA1293Y	1	AG
3-2	Q2	VS2SA1244Y/1E		2SA1244Y	1	AF
3-3	Q3	VS2SA1315Y/1E		2SA1315-Y	1	AC
3-4	Q4, 5	VSFP1A3M///-1	N	FP1A3M (T)	2	AC
3-5	Q6, 7	VSFA1F4M///-1	N	FA1F4M (T)	2	AB
3-6	Q8	VSHN1C01FY/-1	N	HN1C01F-Y (T)	1	AB
3-7	Q9	VS2SA1162SY-1		2SA1162Y	1	AA
4. Diode						
4-1	DA3~9	VHDHN2D01F/-1	N	HN2D01F (T)	7	AC
4-2	DA100~103	VHD1SS181//-1		1SS181	4	AA
4-3	D1~6	VHD1S1885//-1		1S1885	6	AB
4-4	D7, 8	VHDERB81-004/		ERB81-004	2	AE
4-5	D9	VHDERA84-009/		ERA84-009	1	AD
4-6	D10, 11	VHD1SV211//-1	N	1SV211	2	AB
4-7	D12	VHD1SS294//-1		1SS294	1	AA
4-8	ZD1	VHEHZ22-2//-1	N	HZ22-2	1	AA
4-9	ZD2	VHELT1004CZ-1	N	LT1004CZ	1	AM
4-10	LED	RH-PX0186PAZZ	N	LED PR7851K	1	AC
5. Coil						
5-1	L1	RTRNZ0306PAZZ		FERRITE CORE	1	AE
5-2	L2~4	RCILZ3877PAZZ	N	RCR-875D 22μH	3	AE
5-3	L5, 6	RCILZ3880PAZZ	N	RCR-664D 22μH	2	AE
5-4	L7	RCILZ3879PAZZ	N	RCR-664D 270μH	1	AE
5-5	L8	RCILZ3876PAZZ	N	RCR-875D 470μH	1	AE
5-6	L9, 10	RCILZ3878PAZZ	N	RCR-110D 270μH	2	AE
5-7	L11~13	VP-VD101K0000	N	LEM4532 (T)	3	AB
5-8	L14	RCILZ3874PAZZ	N	7KTLT 1.15μH	1	AD
5-9	L15	RCILZ3875PAZZ	N	7KTLT 2.45μH	1	AD
6. Oscillator, Core						
6-1	OSC1	RCRSZ0042PAZZ	N	XTAL 27.8208MHz	1	AN
6-2	OSC2	RCRSZ0041PAZZ	N	XTAL 18.5499MHz	1	AN
6-3	XTL	RCRSZ0043PAZZ	N	XTAL 7.9872MHz	1	AG
6-4	FB1, 2	RCORF0042PAZZ		FERRITE BEAD CORE	2	AB
6-5	FL1~6	RFILN0004PAZZ	N	DSS306-91	6	AB
7. Fuse, Fuse Holder						
7-1	F1, 2	QFS-B0006PAZZ		FUSE (125V/1.25A)	2	AD
7-2		QFSHA2008YAZZ		FUSE HOLDER	4	AA

ELECTRIC PARTS

NO.	REF. NO.	PARTS CODE	NEW	DESCRIPTION	QTY	PRICE
8. Switch, VR						
8-1	SW1	QSW-C0028PAZZ		POWER SWITCH	1	AF
8-2	VR1	RVR-M0232PAZZ	N	CHIP VR 2K	1	AC
8-3	VR2	RVR-M0233PAZZ	N	CHIP VR 50K	1	AF
9. Plug, Connector						
9-1	CN1	QSOCZ0115PAZZ		DC JACK	1	AC
9-2	CN2	QPLGJ0010PAZZ		CONNECTOR (2P) FOR FAN	1	AB
9-3	CN3	QPLGZ0410PAZZ	N	D SUB CONNECTOR (26P)	1	AV
9-4	CN4, 100	QPLGJ0013PAZZ	N	FFC CONNECTOR (6P)	2	AE
9-5	CN5	QPLGZ0409PAZZ	N	MINI DIN CONNECTOR	1	AE
9-6	CN6	QPLGJ0009PAZZ		FFC CONNECTOR (16P)	1	AE
10. Resistor						
10-1	R1~3, 43, 47 125~128, 130	VRS-TW2AD472J		TW)1/10W-4.7KJ	10	AA
10-2	R4~7	RR-TV2AD3302D	N	TV)1/10W-33KD	4	AA
10-3	R8~10	VRS-TW2AD471J		TW)1/10W-470J	3	AA
10-4	R11	VRS-TW2HD621J		TW)1/2W-620J	1	AB
10-5	R12, 13	VRS-TW2ED621J		TW)1/4W-620J	2	AA
10-6	R14, 121, 124, 131~135	VRS-TW2AD223J		TW)1/10W-22KJ	8	AA
10-7	R15	VRS-TW2AD822J		TW)1/10W-8.2KJ	1	AA
10-8	R16, 19	VRS-TW2AD563J		TW)1/10W-56KJ	2	AA
10-9	R17	VRS-TW2AD183J		TW)1/10W-18KJ	1	AA
10-10	R18, 21	VRS-TW2AD243J		TW)1/10W-24KJ	2	AA
10-11	R20	VRS-TW2AD184J		TW)1/10W-180KJ	1	AA
10-12	R22	RR-TV2AD2002D	N	TV)1/10W-20KD	1	AA
10-13	R23	RR-TV2AD4701D	N	TV)1/10W-4.7KD	1	AA
10-14	R24	RR-TV2AD2941D	N	TV)1/10W-2.94KD	1	AA
10-15	R25	RR-TV2AD1502D	N	TV)1/10W-15KD	1	AA
10-16	R26	RR-TV2AD3301D	N	TV)1/10W-3.3KD	1	AA
10-17	R27	RR-TV2AD3242D	N	TV)1/10W-32.4KD	1	AA
10-18	R28	RR-TV2AD4700D	N	TV)1/10W-470D	1	AA
10-19	R29	VRS-TW2AD683J		TW)1/10W-68KJ	1	AA
10-20	R30, 102, 106~108	VRS-TW2AD561J		TW)1/10W-560J	5	AA
10-21	R40	VRS-TW2AD680J		TW)1/10W-68J	1	AA
10-22	R41, 42	VRS-TW2AD823J		TW)1/10W-82KJ	2	AA
10-23	R44, 71	VRS-TW2AD681J		TW)1/10W-680J	2	AA
10-24	R45, 46, 63~68	VRS-TW2AD222J		TW)1/10W-2.2KJ	8	AA
10-25	R60~62	RR-TV2AD75R0D	N	TV)1/10W-75D	3	AA
10-26	R69, 70, 129, 136~146, 161~163, 165~167	VRS-TW2AD103J		TW)1/10W-10KJ	20	AA
10-27	R72	RR-TV2AD9090D	N	TV)1/10W-909D	1	AA

ELECTRIC PARTS

NO.	REF. NO.	PARTS CODE	NEW	DESCRIPTION	QTY	PRICE
10-28	R73	RR-TV2AD7320D	N	TV)1/10W-732D	1	AA
10-29	R74	RR-TV2AD6980D	N	TV)1/10W-698D	1	AA
10-30	R75~78	RR-TV2AD2200D	N	TV)1/10W-220D	4	AA
10-31	R79~98	RR-TV2AD4702D	N	TV)1/10W-47KD	20	AA
10-32	R99, 100, 164	VRS-TW2AD332J		TW)1/10W-3.3KJ	3	AA
10-33	R103~105, 109, 113~120	VRS-TW2AD102J		TW)1/10W-1KJ	12	AA
10-34	R110	VRS-TW2AD331J		TW)1/10W-330J	1	AA
10-35	R111	VRS-TW2AD100J		TW)1/10W-10J	1	AA
10-36	R112	VRD-ST2DF151J		ST)1/5S-150J	1	AA
10-37	R122	VRS-TW2AD470J		TW)1/10W-47J	1	AA
10-38	R123	VRS-TQ2BD106J		TQ)1/8W-10MJ	1	AA
10-39	R147	RR-TV2AD2402D	N	TV)1/10W-24KD	1	AA
10-40	R149	RR-TV2AD4872D	N	TV)1/10W-48.7KD	1	AA
10-41	R150	RR-TV2AD9762D	N	TV)1/10W-97.6KD	1	AA
10-42	R151	RR-TV2AD1963D	N	TV)1/10W-196KD	1	AA
10-43	R153	RR-TV2AD3923D	N	TV)1/10W-392KD	1	AA
10-44	R154	RR-TV2AD7873D	N	TV)1/10W-787KD	1	AA
10-45	R155	RR-TV2AD1584D	N	TV)1/10W-1.58MD	1	AA
10-46	R200, 201	RR-TV2AD1002D		TV)1/10W-10KD	2	AA
11. Capacitor						
11-1	C1, 2	RC-QZS473AFYK		FILM 0.047μF/K/50V	2	AF
11-2	C3, 17, 116~119, 200	VCSATD1CE106M		F93 10μF/16V	7	AD
11-3	C4, 6	VCSATD1EE474M		F93 0.47μF/25V	2	AB
11-4	C5	VCSATD0JE335M		F93 3.3μF/6.3V	3	AB
11-5	C7~9	RC-EZ0184PAZZ	N	RS 470μF/16V	3	AB
11-6	C10~13	RC-EZ0185PAZZ	N	RS 470μF/10V	4	AB
11-7	C14, 15	RC-EZ0186PAZZ	N	RS 220μF/10V	2	AB
11-8	C16	RC-EZ0187PAZZ	N	RS 100μF/25V	1	AB
11-9	C18~20	VCKYTV1HB332K		B/3300pF/K/50V	3	AA
11-10	C21, 22	VCKYTV1HB122K		B/1200pF/K/50V	2	AA
11-11	C23~36, 55~57, 59~61, 91~100, 124~150, 201~203	VCKZTV1EF104Z		F/0.1μF/Z/25V	60	AA
11-12	C37, 101~106	VCCCTV1H3101J		CERAMIC CH/100pF/J/50V	7	AA
11-13	C38, 39	VCSATD1CE225M		F93 2.2μF/16V	2	AC
11-14	C50, 51	RC-QZS103AFYK		FILM 0.01μF/K/50V	2	AF
11-15	C52, 53, 109~115	VCSATH1AE106M		F93 10μF/10V	9	AD
11-16	C54, 151	VCSATH1CE475M		F93 4.7μF/16V	2	AC
11-17	C58, 62	VCKYTV1HB103K		CERAMIC B/0.01μF/K/50V	2	AA
11-18	C70~90, 107, 108, 121	VCSATD1CE105M		F93 1μF/16V	24	AB
11-19	C120	RC-EZ0133PAZZ		JB 27mF/5.5V	1	AF
11-20	C122, 123	VCCCTV1H3180J		CERAMIC CH/18pF/J/50V	2	AA
11-21	C152	VCSATH1AE226M		F93 22μF/10V	1	AD
11-22	C204, 205	VCKYTV1HB102K		CERAMIC B/0.001μF/K/50V	2	AA

CABINET PARTS

NO.	REF. NO.	PARTS CODE	NEW	DESCRIPTION	QTY	PRICE
12-1	①	DCABA0472AASA	N	CABINET ASSEMBLY A	1	BH
12-2	②	DCABB0019AASA	N	CABINET ASSEMBLY B	1	BB
12-3	③	GWAKP0048PASA	N	OPERATION FRAME	1	AE
12-4	④	GDORF0035PASA	N	DOOR	1	AE
12-5	⑤	DFLM-0011PASA	N	ALUMINIUM FRAME ASSEMBLY A	2	AU
12-6	⑥	LFRM-0069PASA	N	ALUMINIUM FRAME C	1	AT
12-7	⑦	PGLSN0013PASA	N	GLASS A	1	BB
12-8	⑧	PGLSN0014PASA	N	GLASS B	1	AT
12-9	⑨	JBTN-0799PASA		KNOB FOR VR	1	AB
12-10	⑩	MSPRP0710PASA	N	RUBBER KEY	1	AD
12-11	⑪	LANGK0973PAZZ	N	ANGLE	1	AE
12-12	⑫	XWHJZ35-05100		POLY SLIDER	1	AA
12-13	⑬	PCUSS0037PAZZ	N	CUSHION SHEET	1	AA
12-14	⑭	RCORF0055PAZZ		TROIDAL CORE	1	AL
12-15	⑮	XNFSD30-24000		NUT M3	1	AA
12-16	⑯	XBPSD30P10000		SCREW 3P+10S	1	AA
12-17	⑰	XBPSD30P06KS0		SCREW 3P+6S	1	AA
12-18	⑱	LX-BZ0216PAZZ		SCREW M3×15	4	AA
12-19	⑲	XYBSF30P10000		SCREW M3×10	9	AA
12-20	⑳	XYBSD30P08000		SCREW M3×8	6	AA
12-21	㉑	XQBSF30P08000		SCREW M3×8	4	AA
12-22	㉒	LX-BZ0215PAZZ		SCREW M3×8	2	AA
12-23	㉓	PSHEF0045PAZZ	N	INSULATION SHEET A	1	AF
12-24	㉔	PSHEM0013PAZZ	N	SHIELD TAPE	1	AK

OTHERS

NO.	REF. NO.	PARTS CODE	NEW	DESCRIPTION	QTY	PRICE
13-1		RRMCG0013PASA	N	REMOTE CONTROL GUN	1	AV
13-2		DADP-0042PAZZ	N	AC ADAPTOR (SEC, SECL)	1	BM
13-3		DADP-0043PAZZ	N	AC ADAPTOR (SEEG)	1	BM
13-4		DSOCZ0063PAZZ	N	9P RGB CABLE	1	BE
13-5		DSOCZ0064PAZZ	N	15P RGB CABLE	1	BH
13-6		QCNW-0133PAZZ	N	6P FLAT CABLE	1	AF
13-7		TINSE0110PAZZ	N	OPERATION MANUAL 〈E〉 (SEC)	1	AQ
13-8		TINSE0111PAZZ	N	OPERATION MANUAL 〈E〉 (SECL)	1	AP
13-9		TINSF0019PAZZ	N	OPERATION MANUAL 〈F〉 (SECL)	1	AP
13-10		TINSL0006PAZZ	N	OPERATION MANUAL 〈E,D,F,I〉 (SEEG)	1	AX
13-11		UBATU0009CEZZ		BATTERY	1	AD
13-12		TLABZ0450PAZZ	N	AC ADAPTOR CAUTION LABEL	1	AB
13-13		PSPAK0052PAZZ	N	LED SPASER	1	AC
13-14		PSHEZ1037ACZZ		SPASER	1	AA

NOT REPLACEMENT ITEM

NO.	REF. NO.	PARTS CODE	NEW	DESCRIPTION	QTY	PRICE
14-1		DPWB-1006PAZZ	N	MAIN P.W.B. ASSEMBLY	1	CZ
14-2		DPWB-1007PAZZ	N	SWITCH P.W.B. ASSEMBLY	1	AY

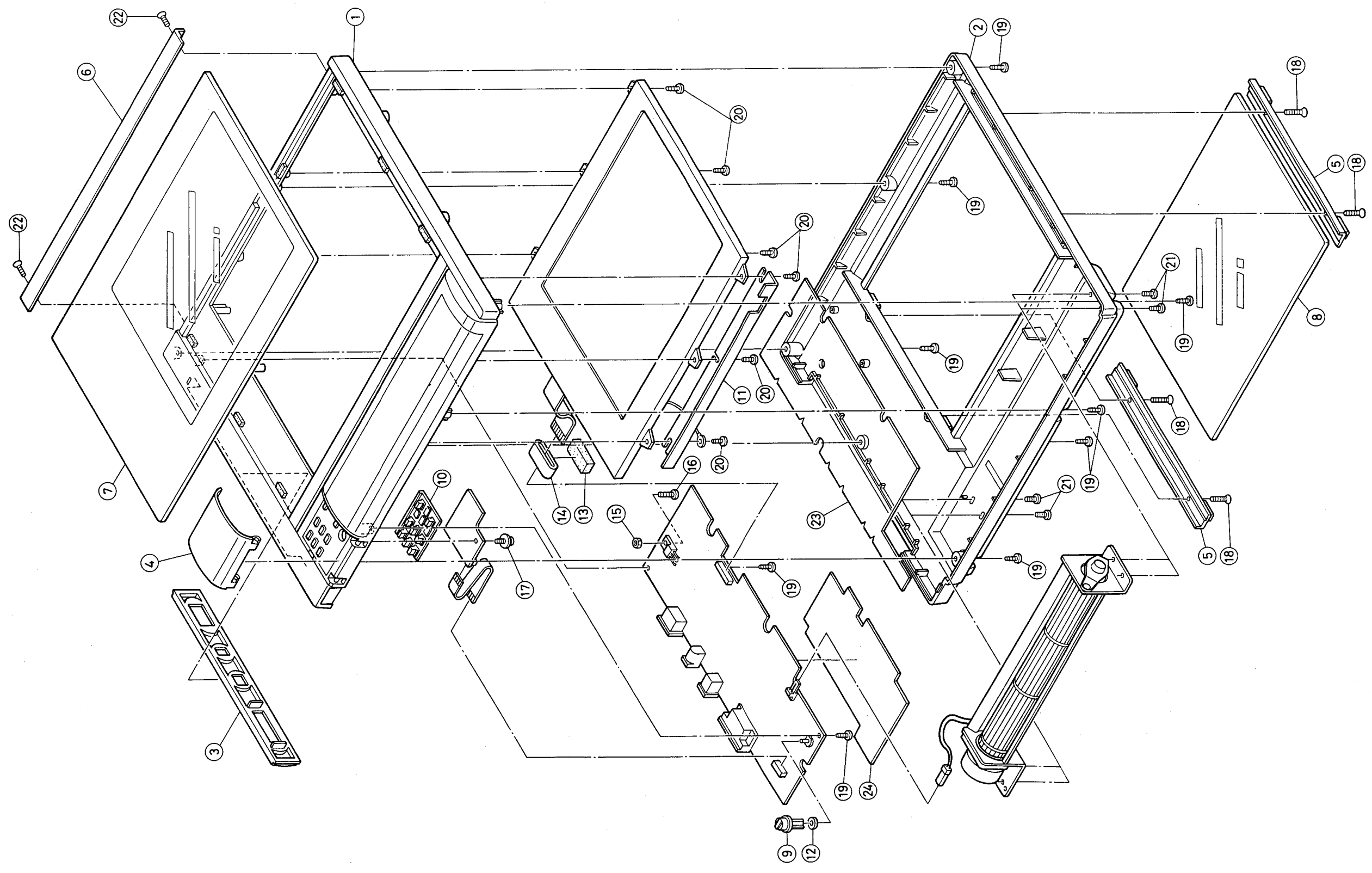


Fig. 43 CABINET PARTS

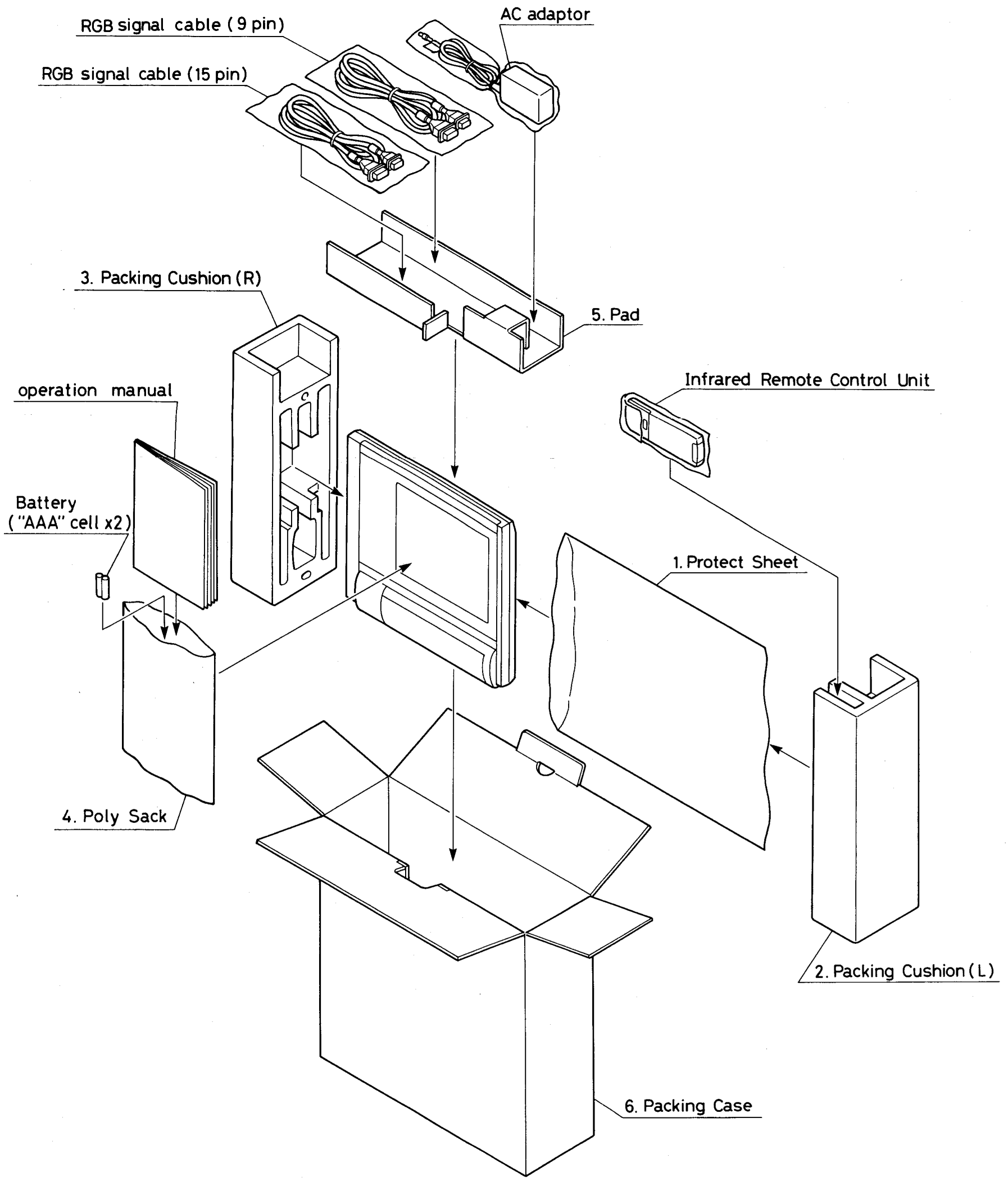
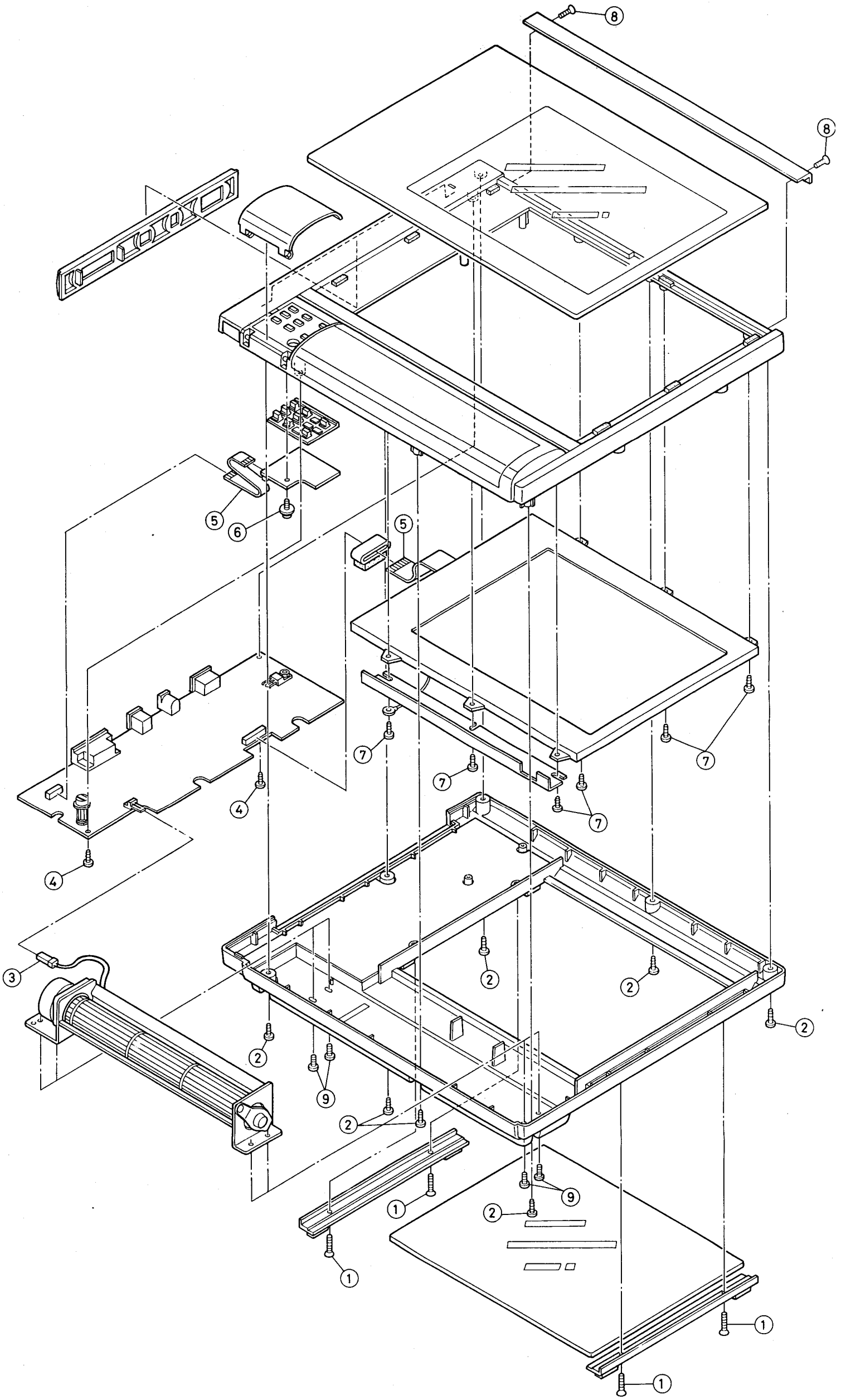


Fig. 44 PACKING OF THE SET

Fig. 45 DISASSEMBLY AND REASSEMBLY



(1) Remove four screws ① holding the aluminium frames.
(2) Remove two aluminium frames and the glass.
(3) Remove seven screws ② holding the top and bottom cabinets.
(4) Separate the top and bottom cabinets and remove the plug ③ from the connector.
(5) Remove the screws ④ holding the main P.W.B. and lift up.
(6) Remove two cables ⑤ from the connectors and remove the main P.W.B.
(7) Remove one screw ⑥ holding the switch P.W.B. and remove it unfolding both sides.
(8) Remove six screws ⑦ holding both the LCD unit and the angle, and remove them.
(9) Remove two screws ⑧ holding the aluminium frame.
(10) Remove the aluminium frame and the glass.
(11) Remove four screws ⑨ holding the fan motor and remove.

INFORMATION

APPLE MAC II Computer has two types of Csync timing signals shown in Fig. 46.
In order to adapt to both signals, the compensational circuit is added on the way. Refer to shading area in Fig. 39.
Therefore, there are three types of P.W.B. pattern (Type A, Type B, Type C) for MAIN P.W.B. ASSEMBLY (DPWB-1006PAZZ) in QA-75.

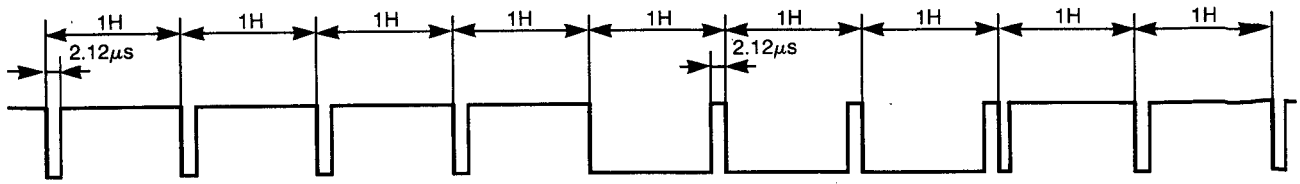
Type A ..... only for "Old Csync". (Fig. 40)
Type B ..... for both "Old Csync" and "Newer Csync". (Fig. 41)
Type C ..... for both "Old Csync" and "Newer Csync". (Fig. 42)

The relation between serial No. and each Type of P.W.B. is approximately as follows.

Destination	Serial No.	Type
for SEC	No. 1 ~ 810, 838, 839, 840	Type A
	No. 811 ~ 2300 except for 838, 839, 840	Type B
	No. 2301 ~	Type C
for SECL	No. 1 ~ 350	Type B
	No. 351 ~	Type C
for SEEG	No. 1 ~	Type C
service parts		Type B or C

If the display is abnormal when APPLE MAC II signal is inputed to Type A P.W.B., the MAIN P.W.B. ASSEMBLY should be replaced with Type B or Type C.

① Newer Csync



② Old Csync

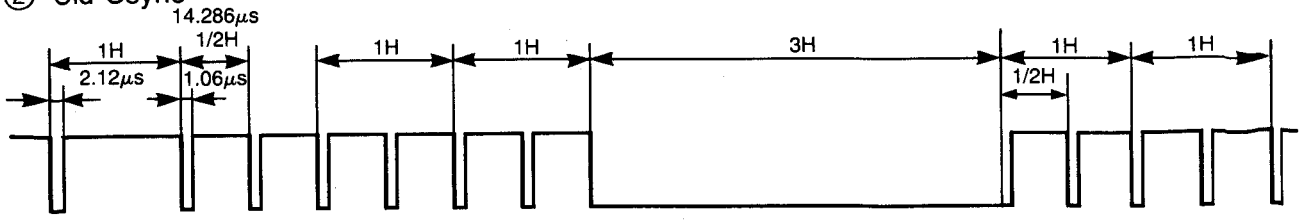
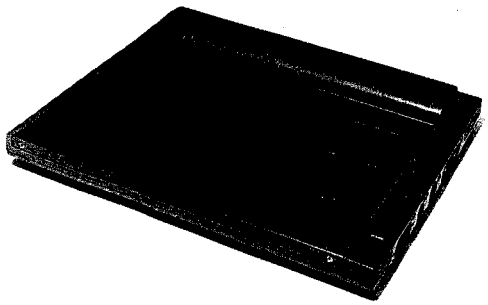


Fig. 46

SHARP

SERVICE MANUAL

S8214QA-75A/



COMPUTER PROJECTION PANEL

MODEL QA-75A

In the interests of user-safety (Required by safety regulation in some countries), the set should be restored to its original condition and only parts identical to those specified should be used.

This Service Manual was prepared to show the differences between the QA-75A and the QA-75.
For all other service information, refer to the Service Manual for the QA-75.

SHARP CORPORATION

1.SPECIFICATIONS

The contrast ratio is improved from 17:1 to 20:1.
(Refer to page.2 in the QA-75 Service Manual.)

2.TROUBLESHOOTING CHART

TP4(V_{EE})≒ -17.0± 1.0V(Refer to page.47 in the QA-75 Service Manual.)

3.CIRCUIT DIAGRAM & P.W.B.

The CIRCUIT DIAGRAM is changed.(Refer to attached CIRCUIT DIAGRAM and Table 1.)

4.REPLACEMENT PARTS LIST

Shown below are the parts different between models QA-75 and QA-75A.

Table 1

			QA-75	QA-75A		
page	REF.No.		Part No.	Part No.	Description	Price
65	1-1	-	DUNTL0052PAZZ	DUNTL2084YAZZ	LCD UNIT(LM64N662)	CM
67	10-16	R26	RR-TV2AD3301D	RR-TV2AD2491D	TV)1/10W-2.49KD	AA
68	10-39	R147	RR-TV2AD2402D	VRN-TV2AQ393D	TV)1/10W-39KD	AA
68	10-40	R149	RR-TV2AD4872D	VRN-TV2AQ823D	TV)1/10W-82KD	AA
68	10-41	R150	RR-TV2AD9762D	VRN-TV2AR154D	TV)1/10W-150KD	AA
68	10-42	R151	RR-TV2AD1963D	VRN-TV2AR334D	TV)1/10W-330KD	AA
68	10-43	R153	RR-TV2AD3923D	VRN-TV2AR684D	TV)1/10W-680KD	AA
68	10-44	R154	RR-TV2AD7873D	VRS-TW2AD155J	TW)1/10W-1.5MJ	AA
68	10-45	R155	RR-TV2AD1584D	VRS-TW2AD305J	TW)1/10W-3MJ	AA
69	12-7	-	PGLSN0013PASA	PGLSN2006YASA	GLASS A	BB
70	13-4	-	DSOCZ2004YAZZ	DSOCZ2021YAZZ	9P RGB CABLE(SEEG)	BF
70	13-1	-	RRMCG0013PASA	RRMCG0030PASA	REMOTE CONTROL UNIT	AV
70	13-7	-	TINSE0110PAZZ	TINSE2043YAZZ	OPERATION MANUAL<E>(SEC)	AQ
70	13-8	-	TINSE0111PAZZ	TINSE2046YAZZ	OPERATION MANUAL<E>(SECL/SCA)	AP
70	13-9	-	TINSF0019PAZZ	TINSF2047YAZZ	OPERATION MANUAL<F>(SECL/SCA)	AP
70	13-10	-	TINSL0006PAZZ	TINSL2044YAZZ	OPERATION MANUAL<E,D,F,I>(SEEG)	AX
-	-	-	TINSE2026YAZZ	TINSE2045YAZZ	OPERATION MANUAL<E>(SUK)	AQ
70	14-1	-	DPWB-1006PAZZ	DPWB-2072YAZZ	MAIN P.W.B. ASSEMBLY(SEC/SECL/SCA)	CZ
*(1)	7-2	-	DPWB-1030PAZZ	DPWB-2073YAZZ	MAIN P.W.B. ASSEMBLY(SEEG/SUK)	CZ
-	-	-	Not used	RCORF2013YAZZ	CRAMP CORE FOR AC ADAPTOR(SEEG)	AP

*(1) : Refer to supplement manual in the QA-75 Service Manual.

○ The circled resisters are changed.

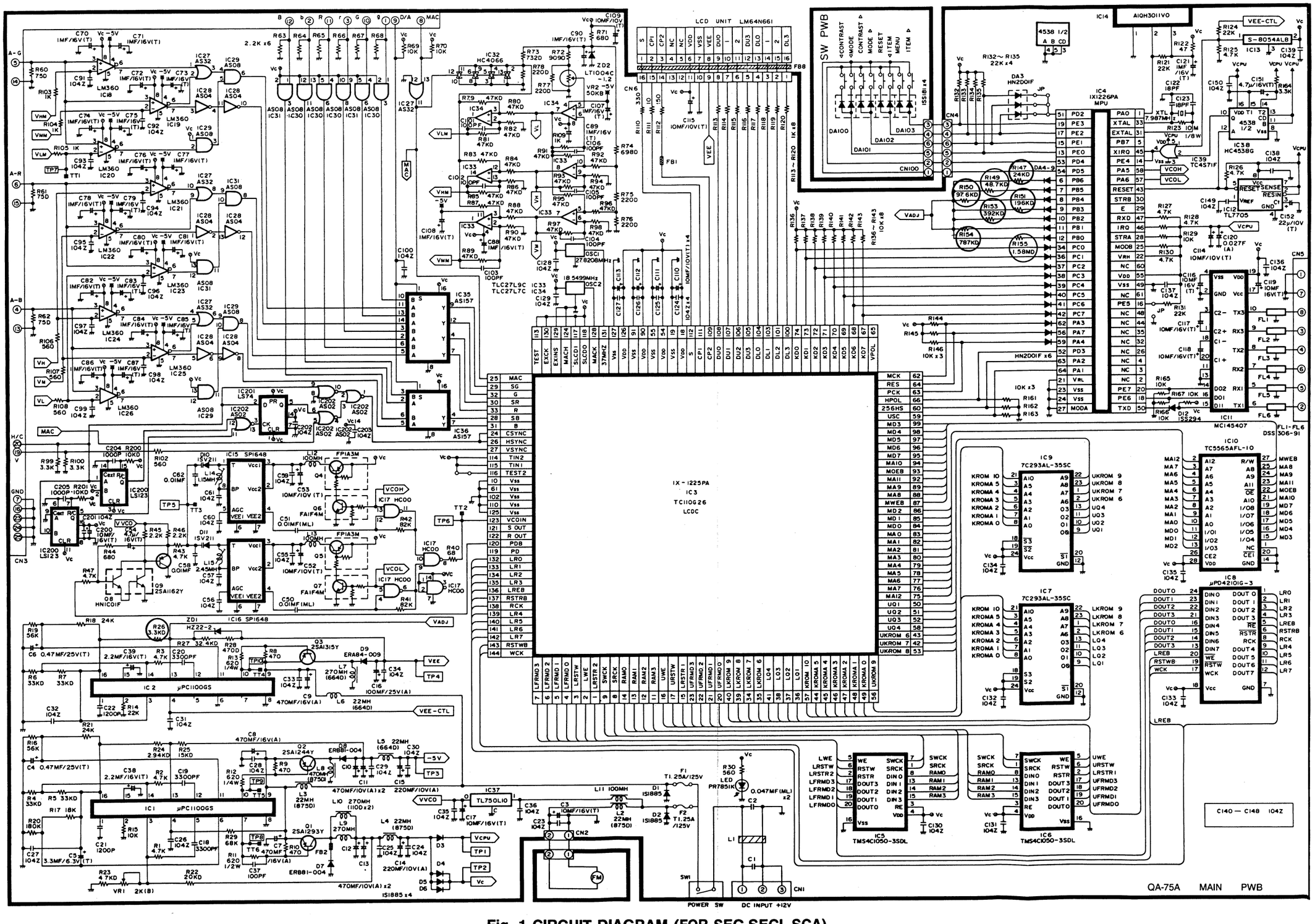


Fig. 1 CIRCUIT DIAGRAM (FOR SEC,SECL,SCA)

○ The circled resisters are changed.

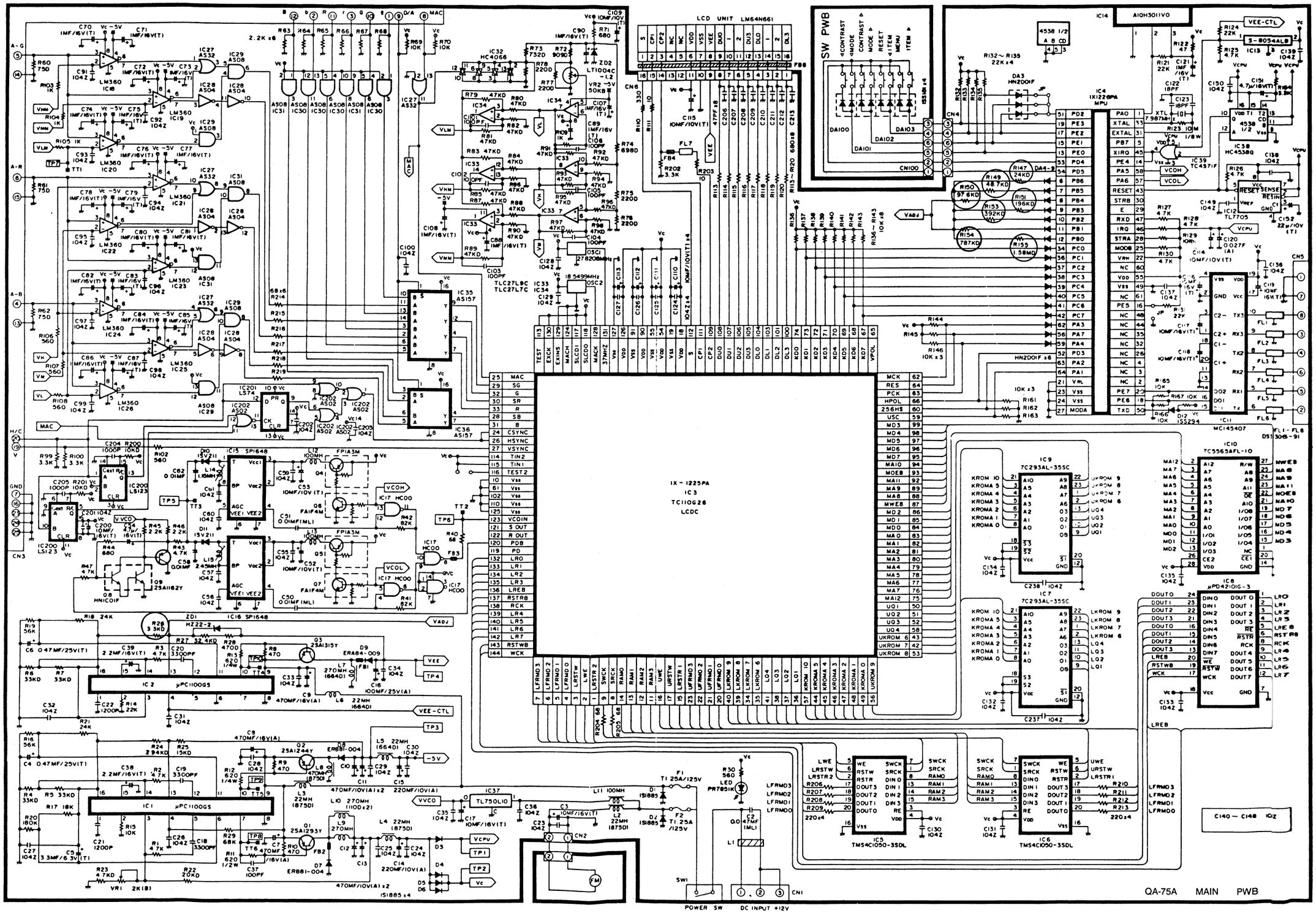


Fig. 2 CIRCUIT DIAGRAM (FOR SEEG SUK)